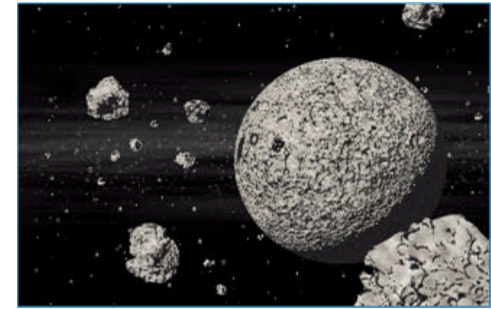


# Asteroid-Z MS-7423N1

Version 10



## CPU:

Wolfdale, Conroe, Conroe-1M,  
; TDP max=65W, FSB 1333/1066/800

## System Chipset:

Intel Q45 (North Bridge)  
Intel ICH10DO (South Bridge)

## On Board Chipset:

BIOS -- SPI FLASH 32MB  
HD AUDIO Codec -- ALC262  
LPC Super I/O -- SMSC SCH5617  
LAN --INTEL 82567LM Boazman  
Clock GEN-IDTCV184-2  
TPM - SLB9635 TT1.2  
PCMCIA - Ricon 5C812/PCI

## Expansion Slots:

Half mini PCIE SLOT \* 1

## Main Memory:

DDR III \* 2 - 1066 w/o ECC

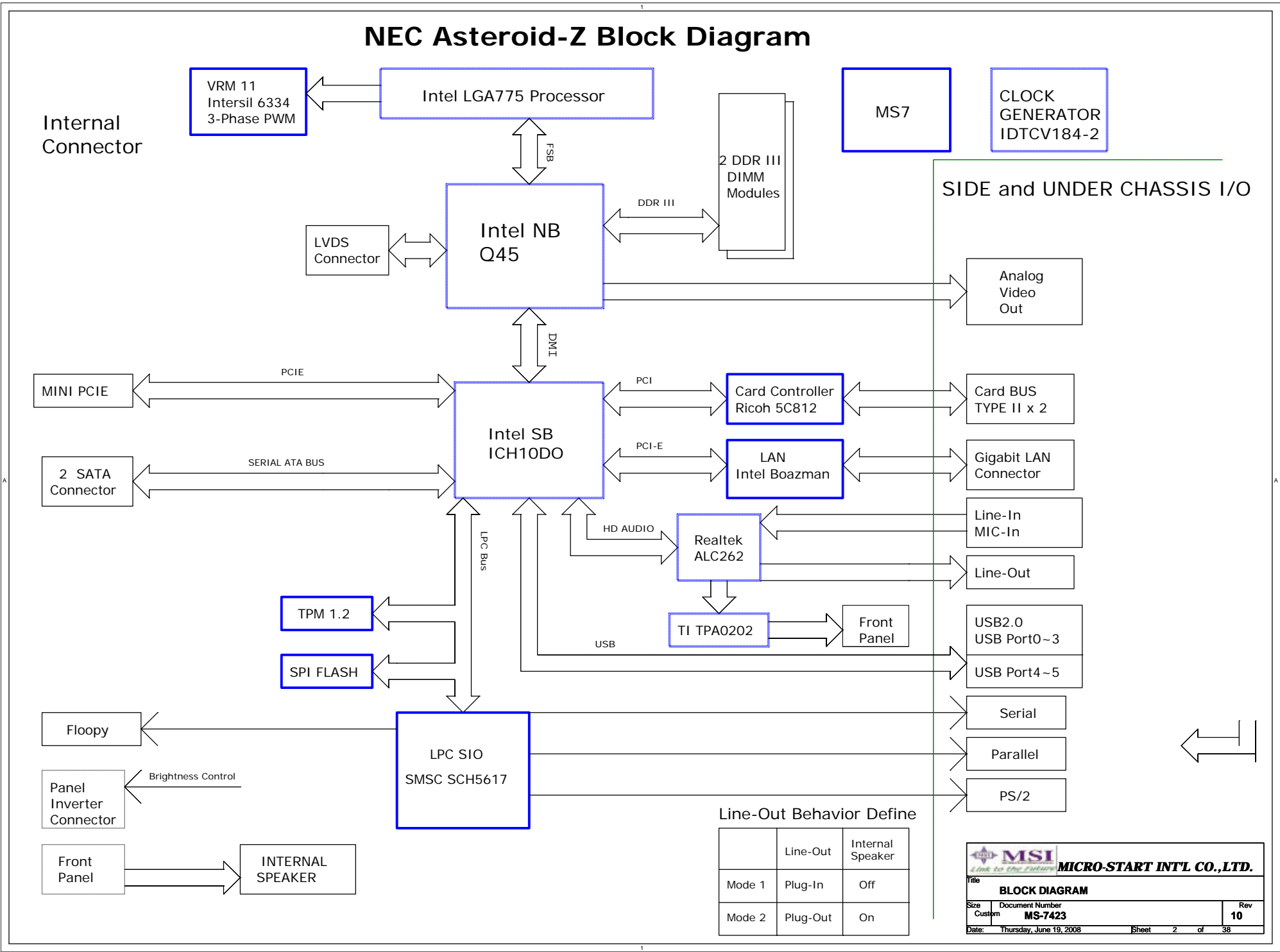
## Intersil PWM:

Controller: Intersil 6334 3Phase

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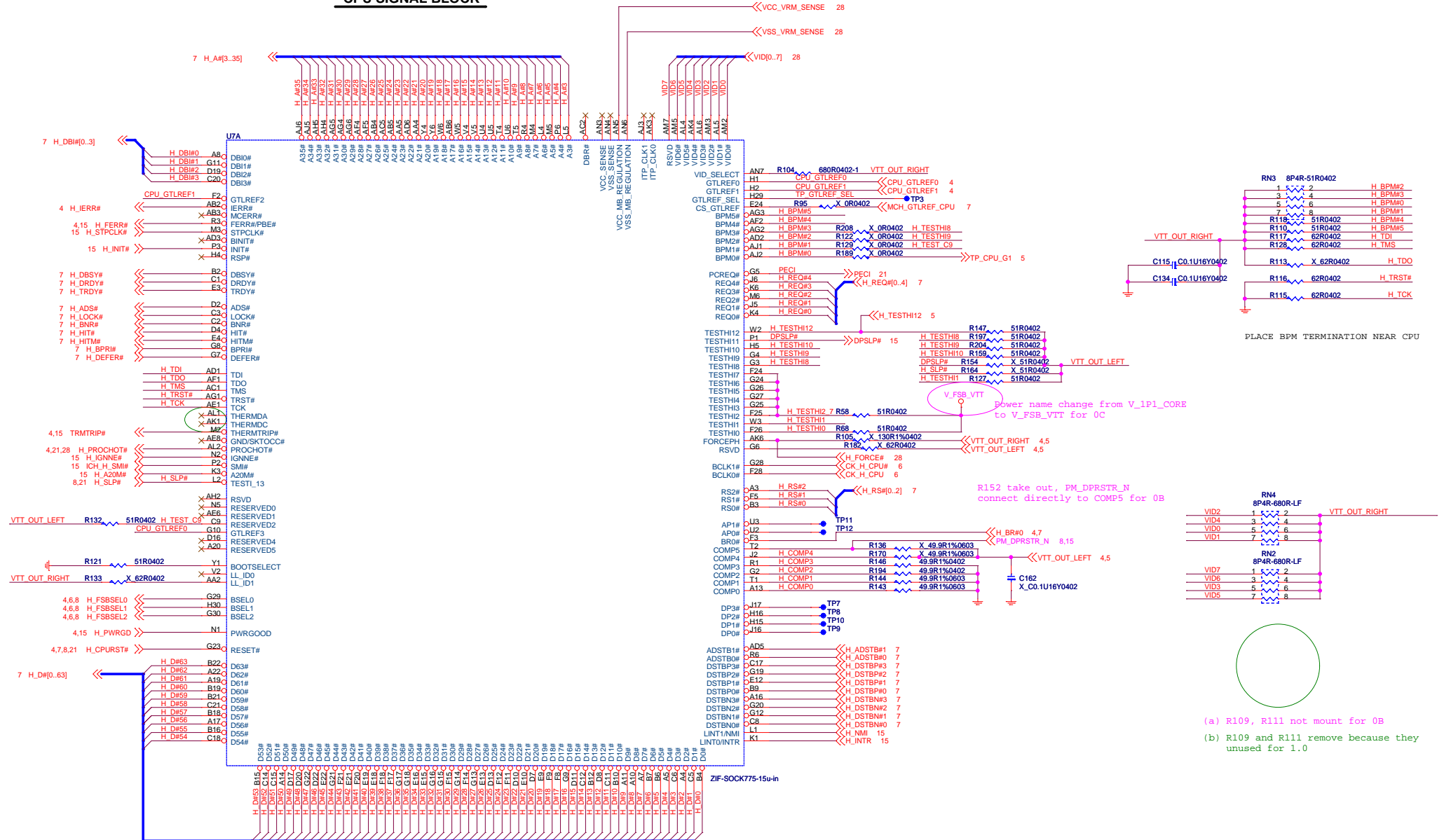


NEC Asteroid-Z Block Diagram





### CPU SIGNAL BLOCK



BSEL			TABLE
2	1	0	FSB FREQUENCY
0	0	0	267 MHZ (1067)
0	1	0	200 MHZ (800)
0	0	1	133 MHZ (533)
1	0	0	333 MHZ (1333)







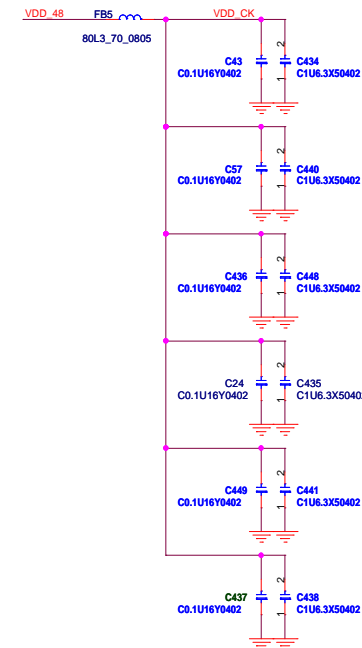
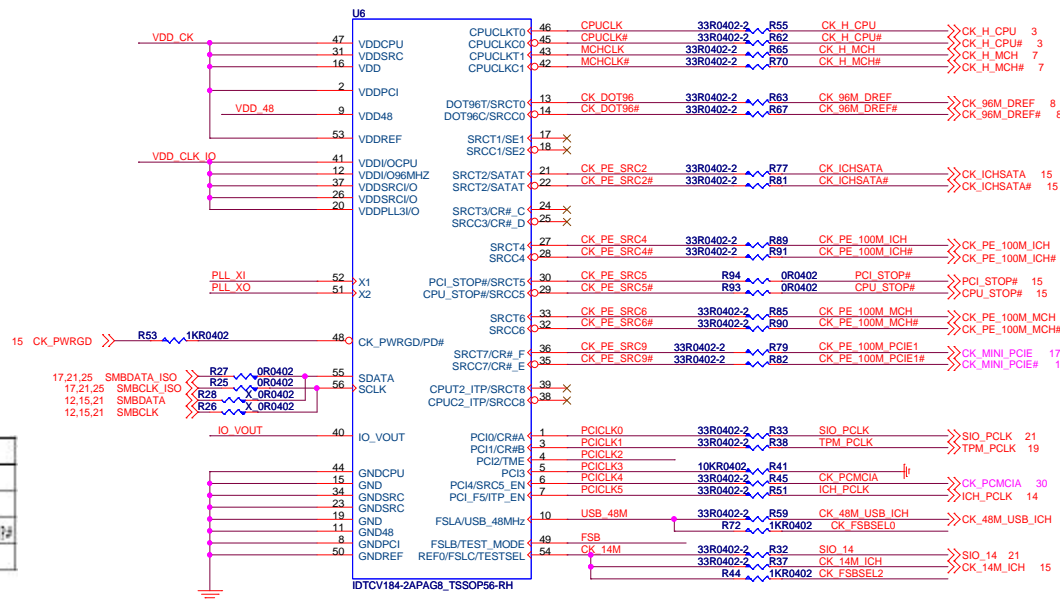




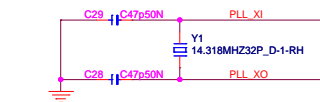
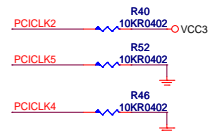
# CLOCK Generator - IDTCV184-2

## VDD\_CK Decoupling

Place near each VDD\_CK Pins

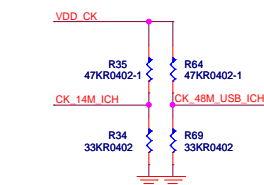
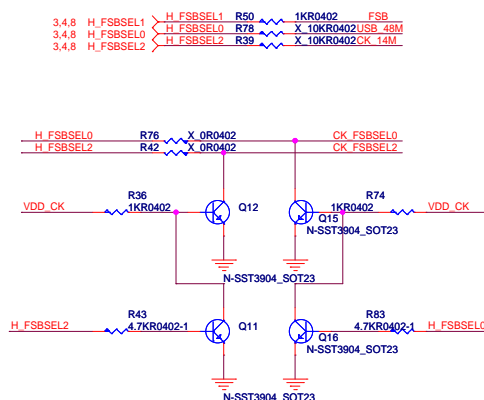


## Strapping resistor



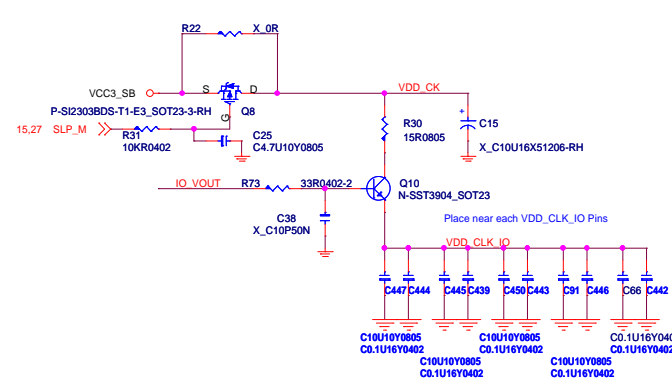
C28, C29 are changed from 27pF to 47pF for 0B

## CPU Frequency select

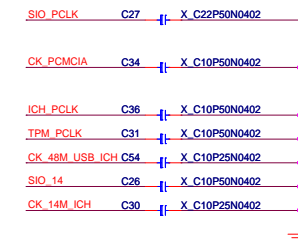


FS <sub>0</sub> C <sup>1</sup> B0b7	FS <sub>0</sub> B <sup>1</sup> B0b6	FS <sub>0</sub> A <sup>2</sup> B0b5	CPU MHz
0	0	0	266.66
0	0	1	133.33
0	1	0	200.00
0	1	1	166.66
1	0	0	333.33
1	0	1	166.66
1	1	0	400.00
1	1	1	Reserved

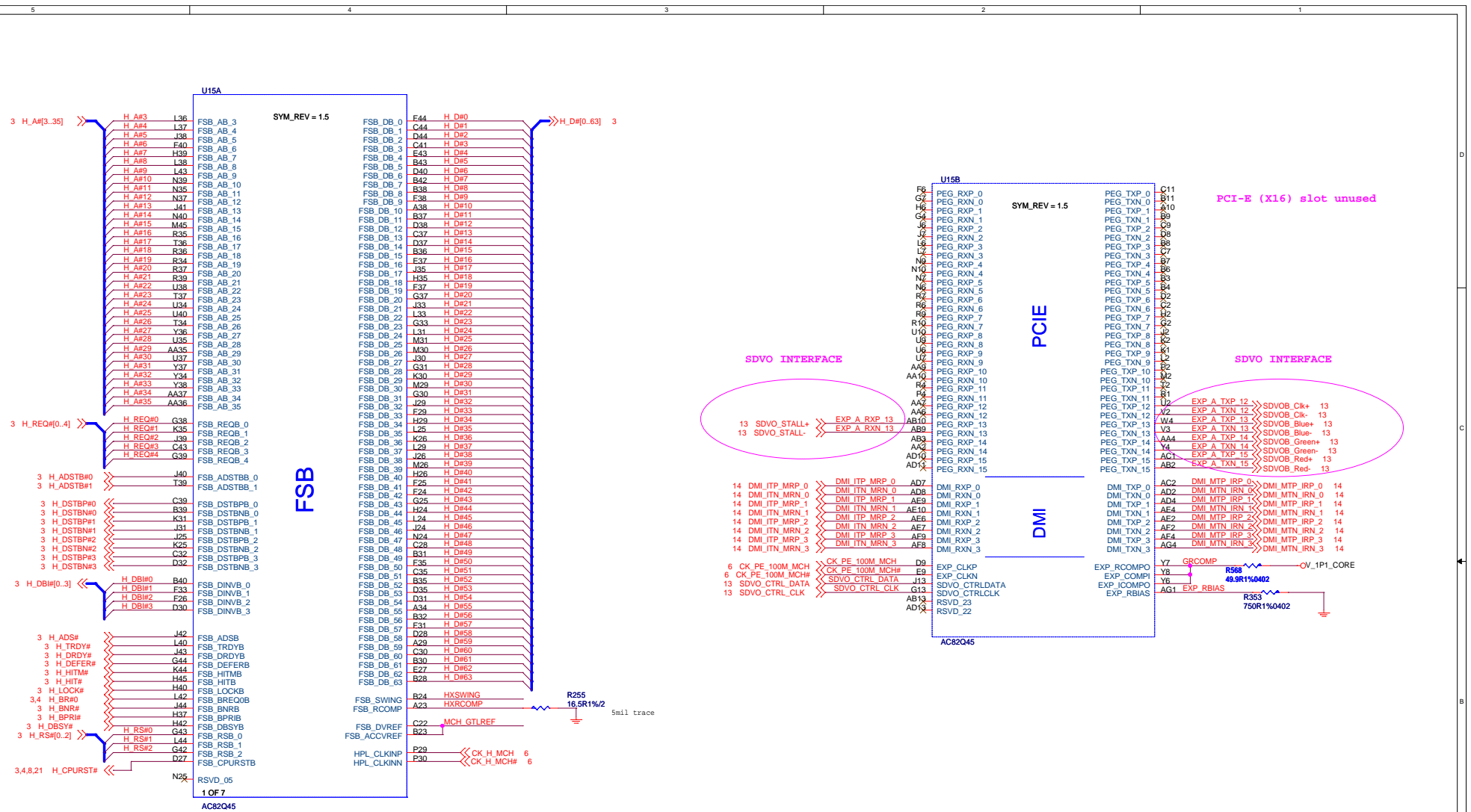
## VDD\_CK & VDD\_CLK\_IO Power



## For EMI reserver

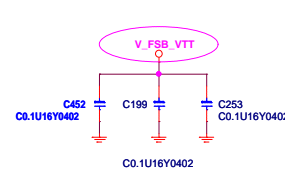
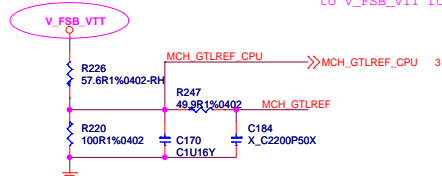
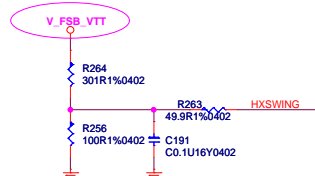




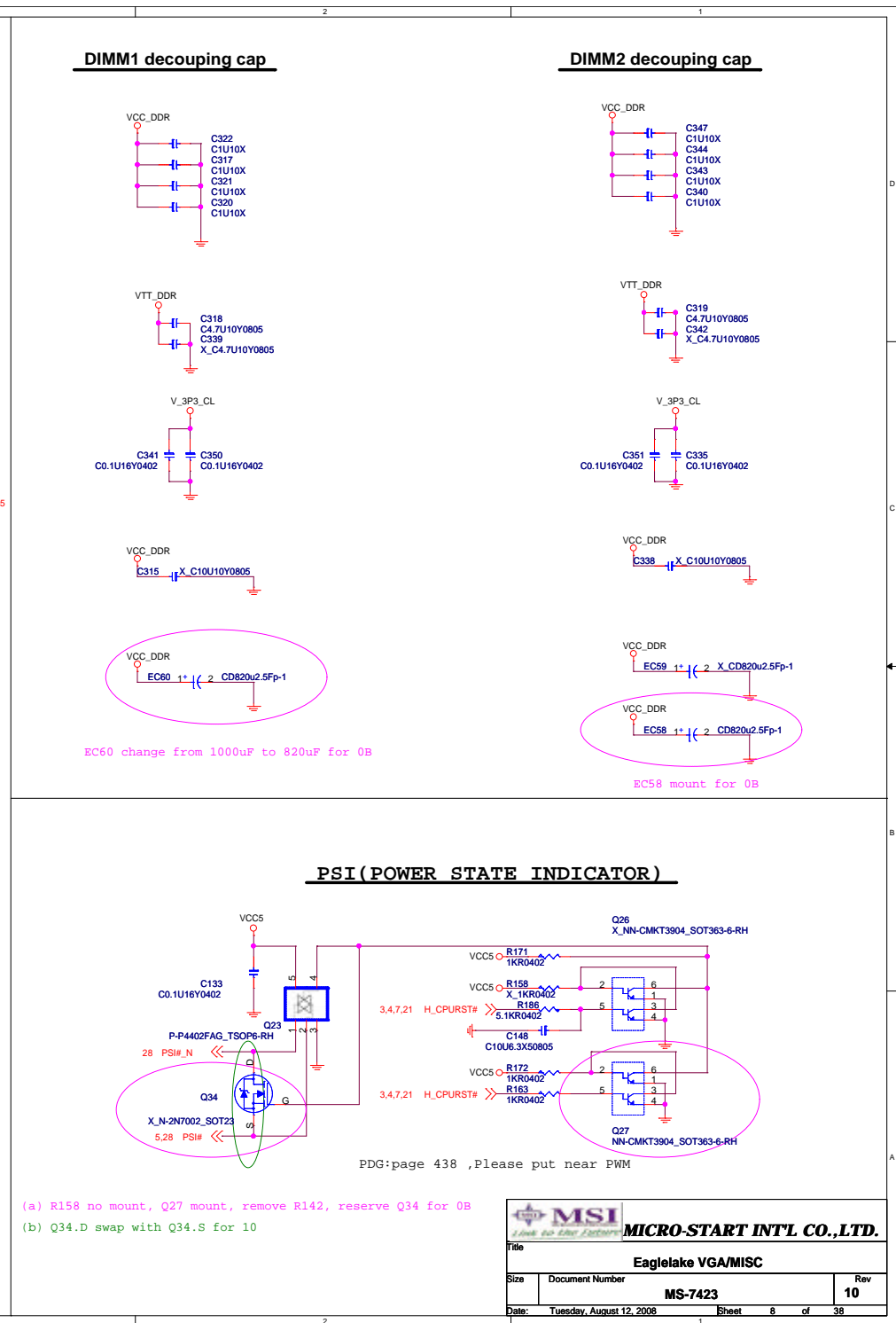
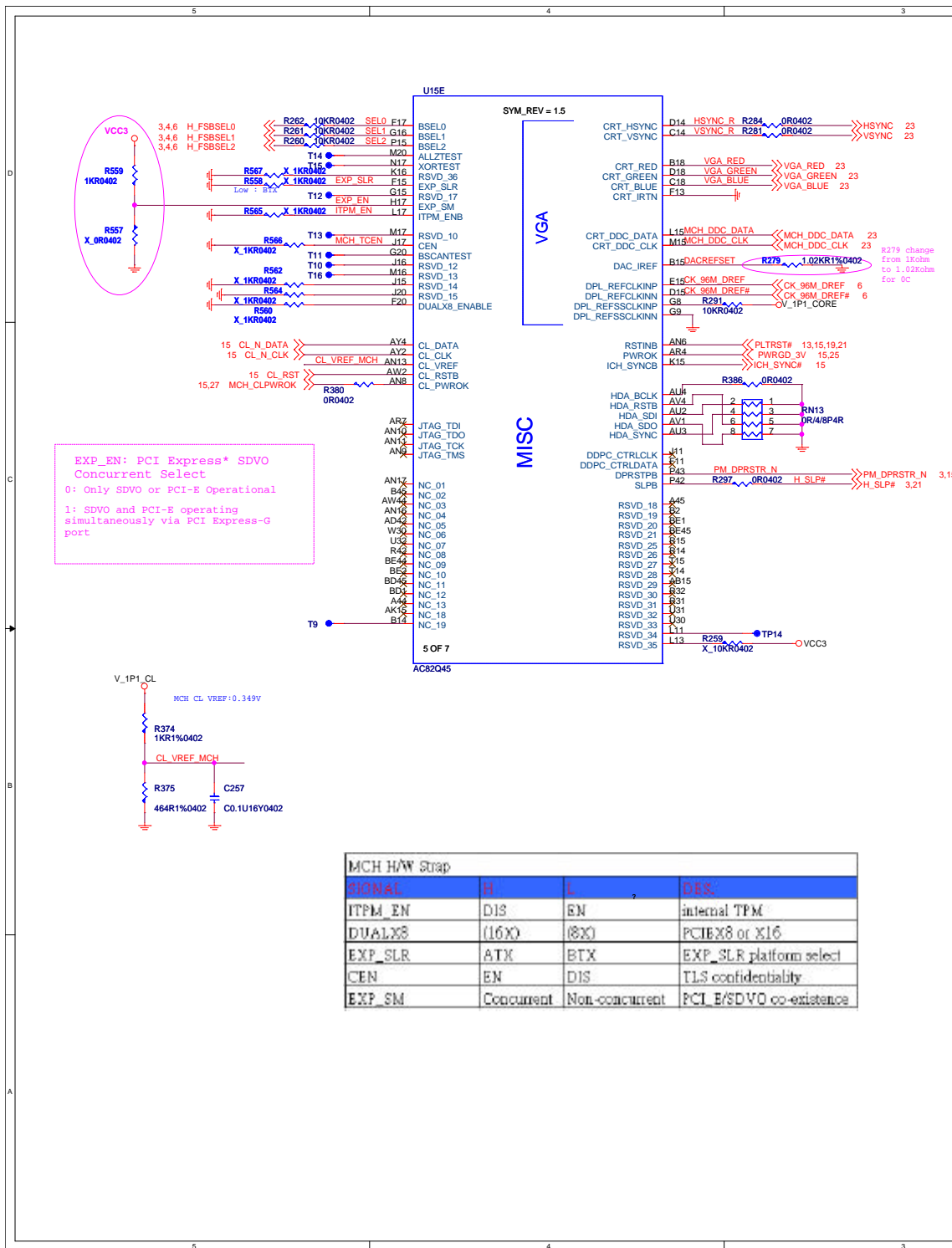


HD\_SWING VOLTAGE \*10 MIL TRACE , 7 MIL SPACE\* HD\_SWING S/B 1/4\*VTT +/- 2%

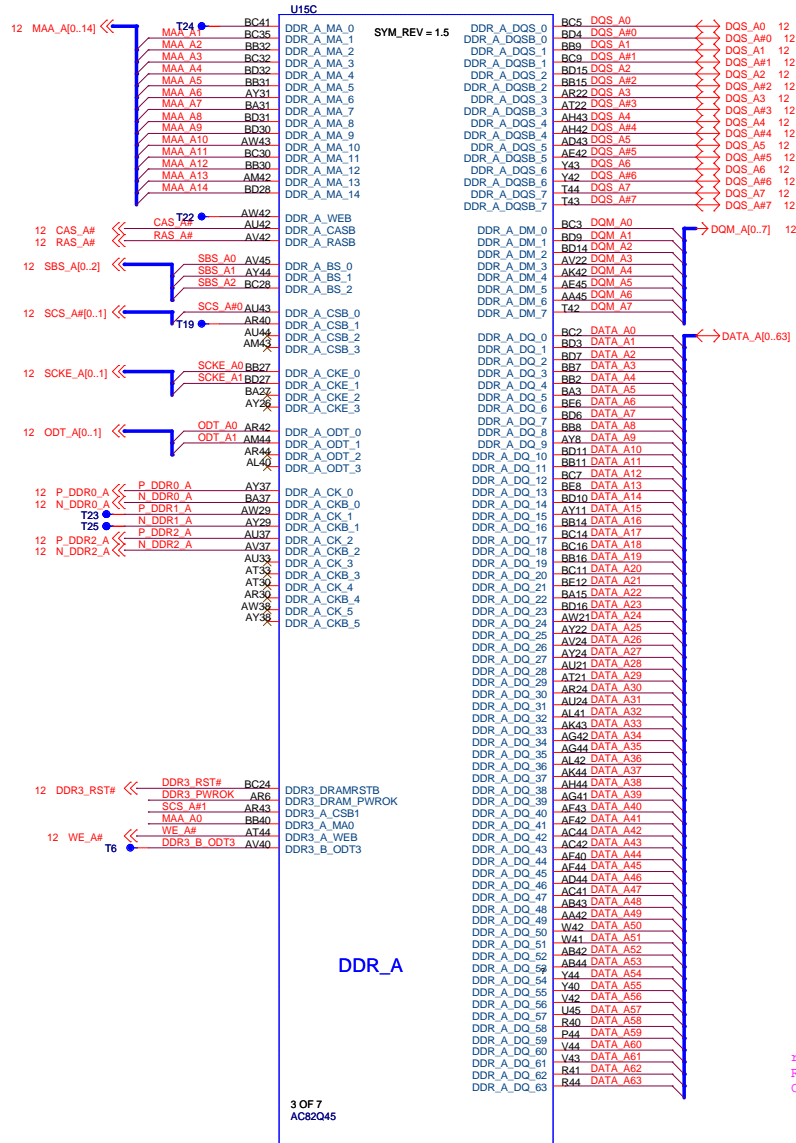
PLACE DIVIDER RESISTOR NEAR VTT





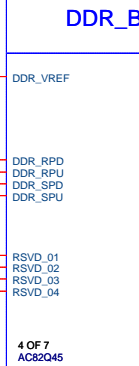
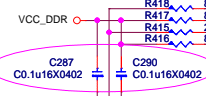
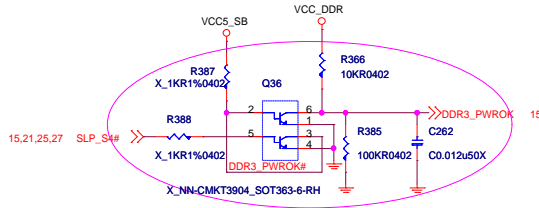
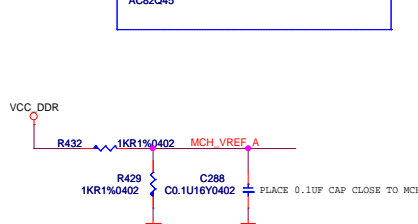




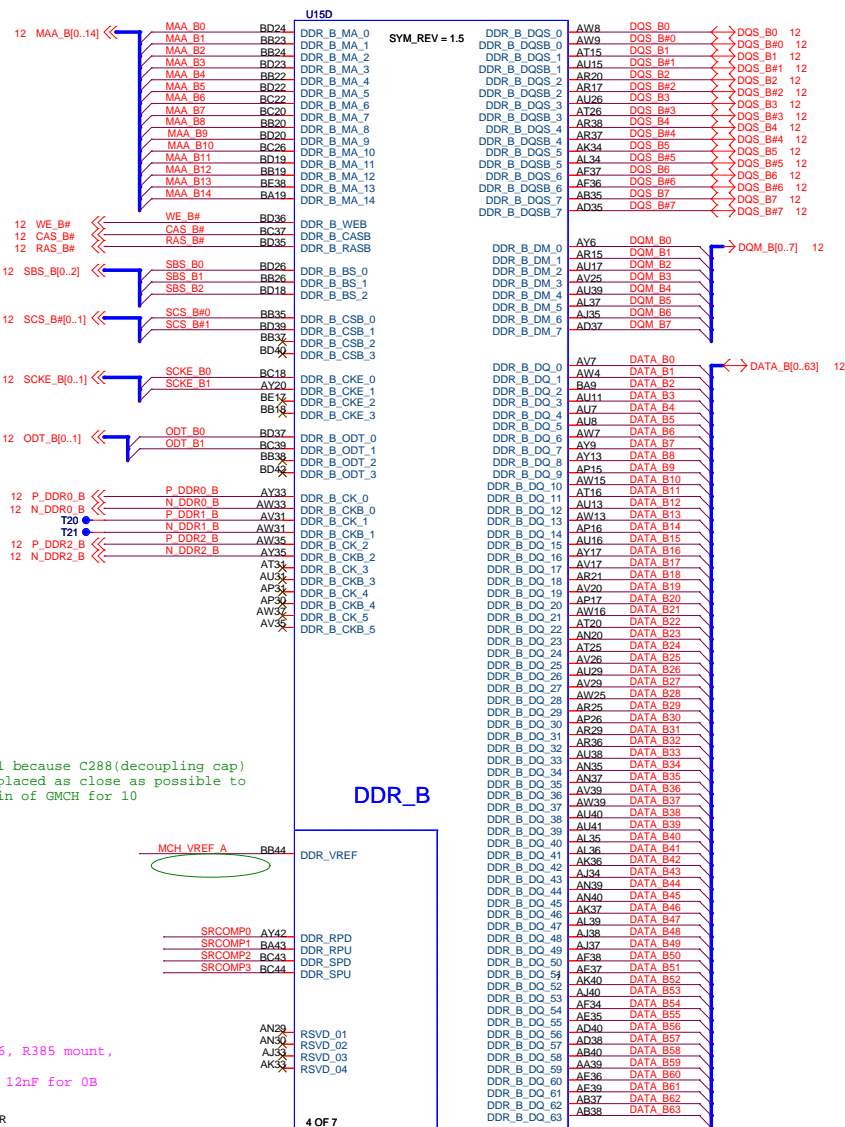


remove C291 because C288(decoupling cap)  
should be placed as close as possible to  
DDR\_VREF pin of GMCH for 10

remove Q54, Q56, add Q36, R385 mount,  
R387& R388 not mount  
C262 change from 1uF to 12nF for 0B



C287 change from Y5V to X7R;  
C290 change from 0603 type/Y5V to 0402 type/X7R for 0B



MSI  
MICRO-START INT'L CO.,LTD.

Eaglelake Memory

MS-7423

Rev 10

Date: Tuesday, August 12, 2008

Sheet 9 of 38



# POWER

Power name change from  
V\_1P1\_CORE to  
V\_FSB\_VTT for 0C

V\_FSB\_VTT

V\_1P1\_CORE

U15F

SYM-REV: 1.1.0

AA19

AA23

AA25

AA27

AA29

AA30

AA32

AA34

AA36

AA38

AA40

AA42

AA44

AA46

AA48

AA50

AA52

AA54

AA56

AA58

AA60

AA62

AA64

AA66

AA68

AA70

AA72

AA74

AA76

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AA664

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AA668

AA670

AA672

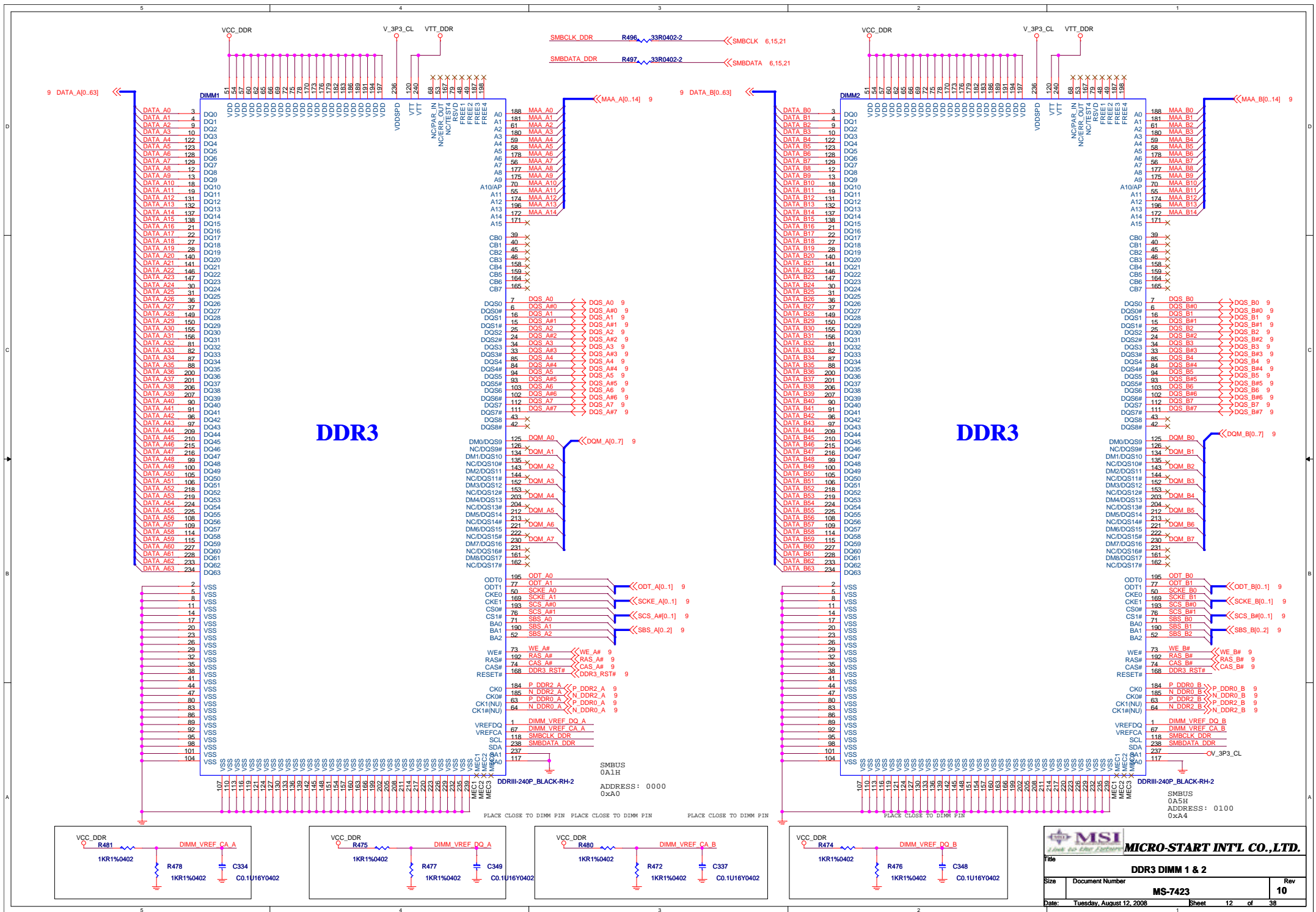
AA674

AA676











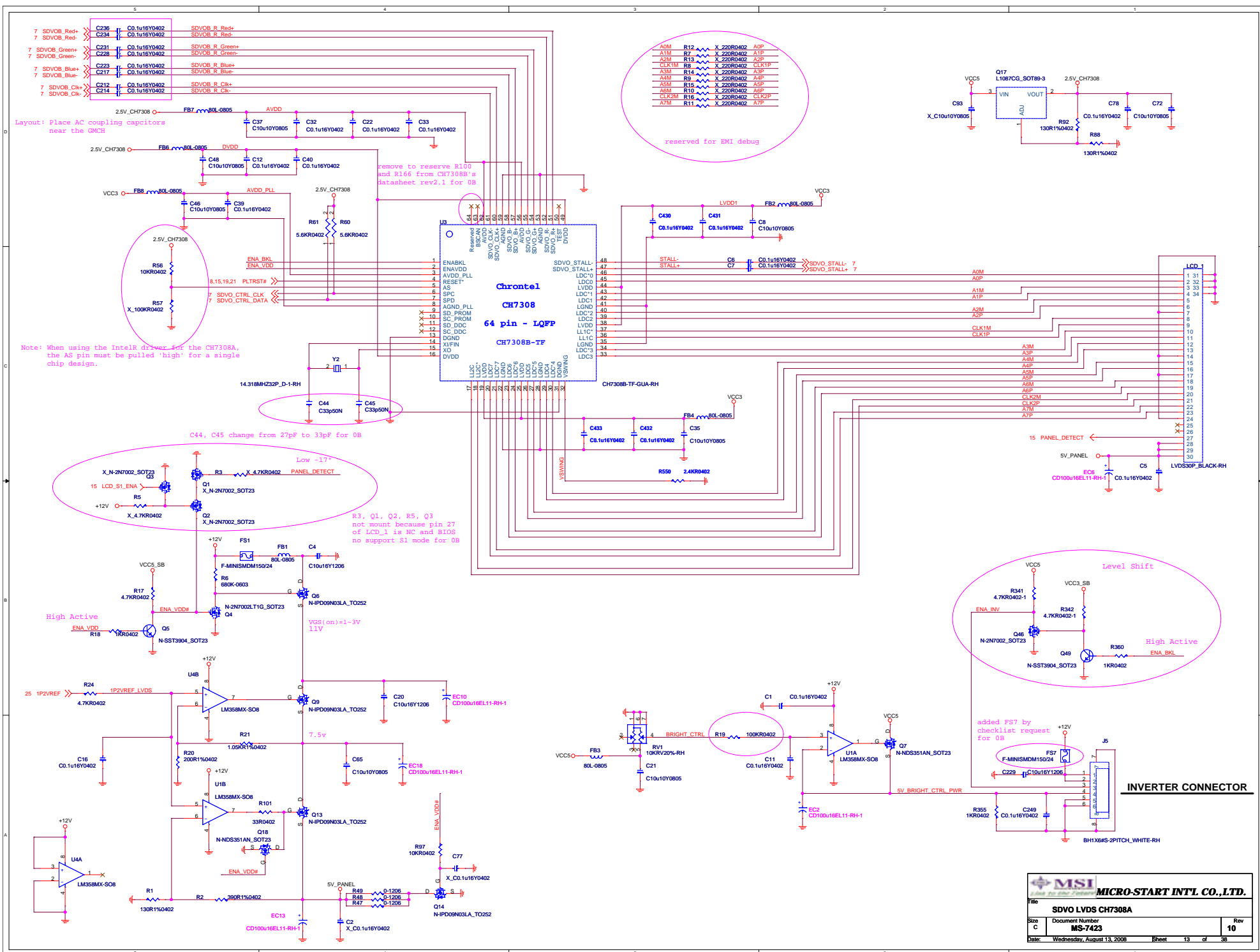




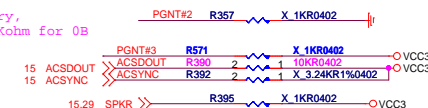
Figure 10 shows the pin connections for the P4R-8.2K0402-LF. The connections are as follows:

- Header 1 (Top):**
  - Pin 1: VCC#3
  - Pin 2: P4R-2.7K0402-LF (RN11)
  - Pin 3: P4R-2.7K0402-LF (RN12)
  - Pin 4: VCC#3
- Header 2 (Middle):**
  - Pin 5: P4R-2.7K0402-LF (RN11)
  - Pin 6: P4R-2.7K0402-LF (RN12)
  - Pin 7: P4R-2.7K0402-LF (RN16)
  - Pin 8: VCC#3
- Header 3 (Bottom):**
  - Pin 9: P4R-8.2K0402-LF (RN14)
  - Pin 10: P4R-8.2K0402-LF (RN15)
  - Pin 11: P4R-8.2K0402-LF (RN15)
  - Pin 12: P4R-8.2K0402-LF (RN15)
- Header 4 (Bottom):**
  - Pin 13: P4R-8.2K0402-LF (RN15)
  - Pin 14: P4R-8.2K0402-LF (RN15)
  - Pin 15: P4R-8.2K0402-LF (RN15)
  - Pin 16: P4R-8.2K0402-LF (RN15)

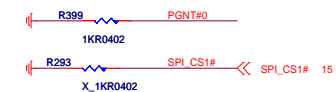


ICH10 H/W STRAPS			
SIGNAL	H	L	DES.
SPKR	DIS	EN	REBOOT
GNT3	DIS	EN	A16 OVERRIDE
INTVRMEN	EN	DIS	INT VRM
SATALED	NORM	REVERSE	PCIE 0-3 ORDER
HDA_SDOUT	EN	DIS	Danbury Tec.
HDA_SYNC	SET BIT	N/A	PCIE PORT CONFIG BIT 0 (1-4)
GNT2	N/A	SET BIT	PCIE PORT CONFIG 2 BIT 0 (5-6)

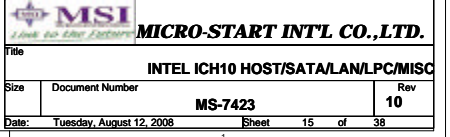
Support Danbury,  
R390 mount 10Kohm for 0B



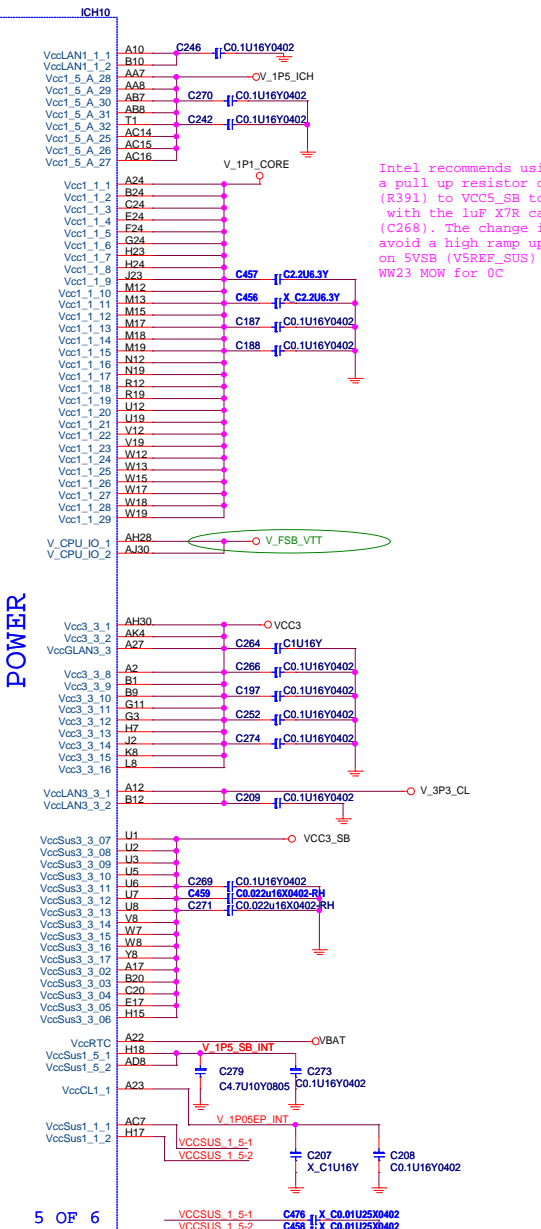
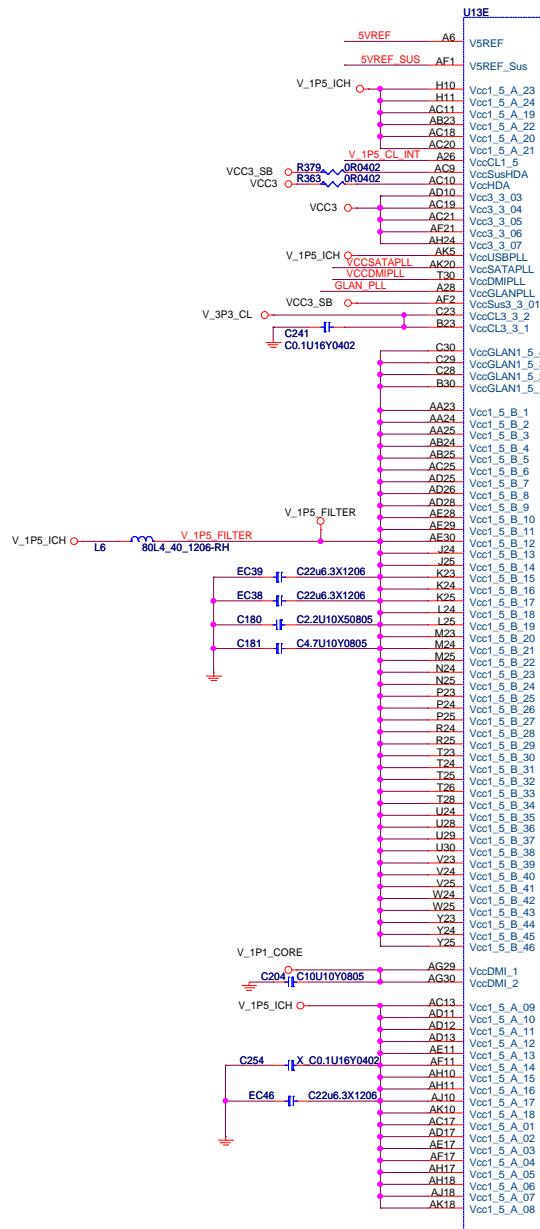
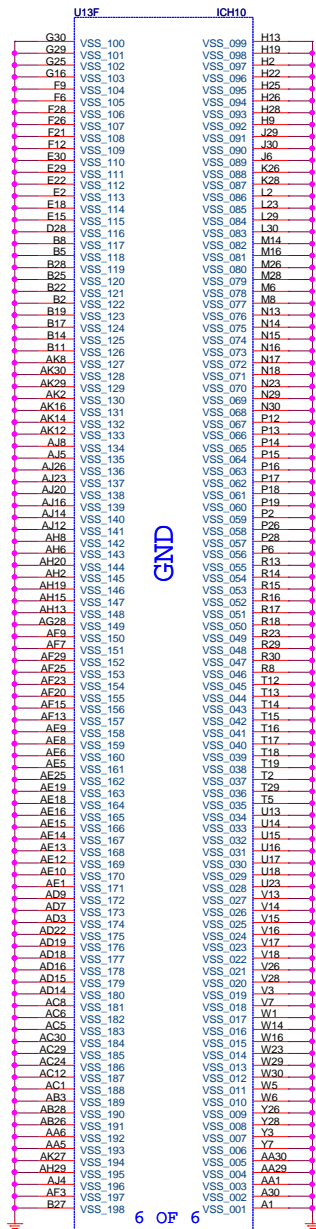
BOOT SELECT STRAPS			
BOOT DEVICE	GNT#0	SPI_CS1#	
FWH	1	1	
SPI	0	X	(Default)
PCI	1	0	



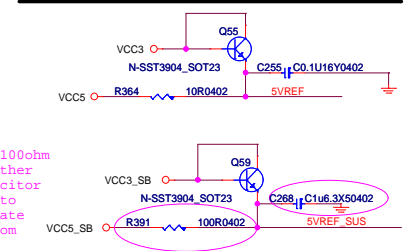




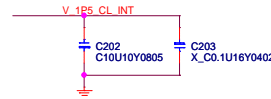




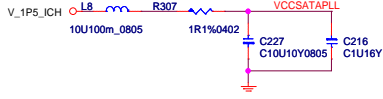
# 5VREF & 5VREF\_SUS Sequencing Circuit



## V\_1P5\_CL decoupling



## VCCSATAPLL



## VCCDMIPLL



## GLAN\_PLL

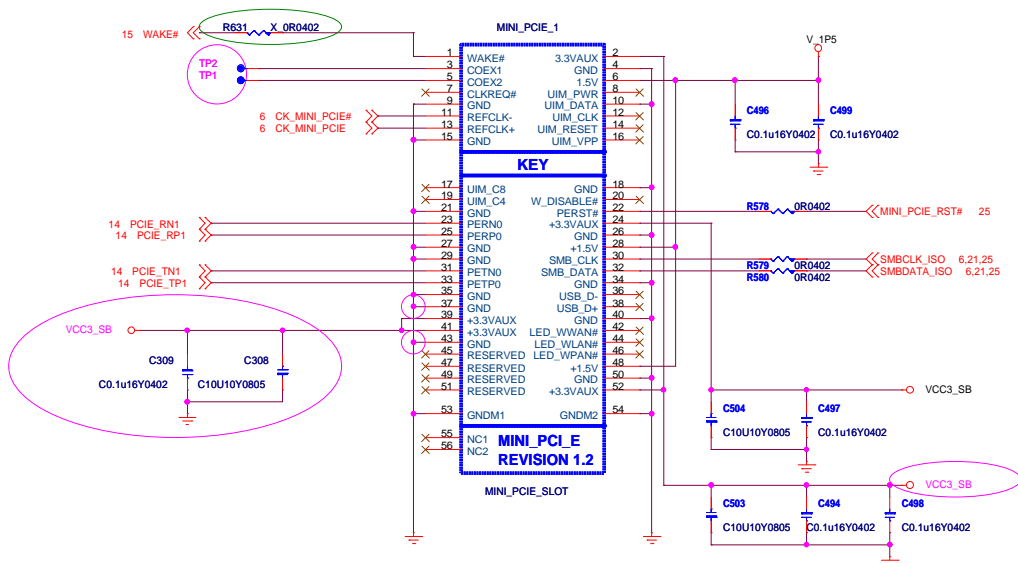


Intel recommends using a pull up resistor of 100ohm (R391) to VCC5\_SB together with the 1uF X7R capacitor (C268). The change is to avoid a high ramp up rate on 5VSB (V5REF\_SUS) from WW23 MOW for 0C

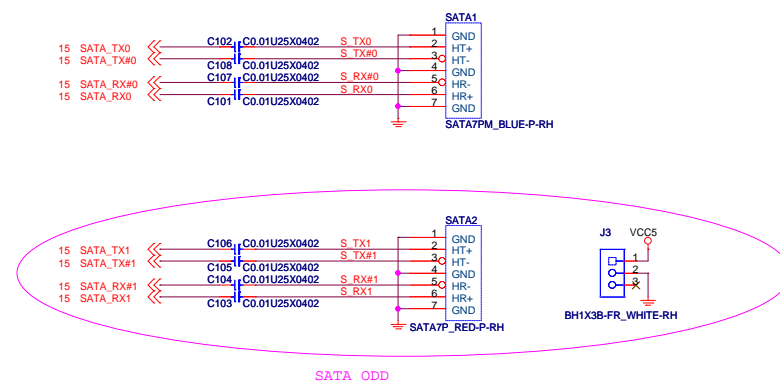


## MINI PCI-E BLOCK

Reversed R631 by customer request because Asteroid-Z doesn't support WOL on WLAN card for 1.0 on 8/5

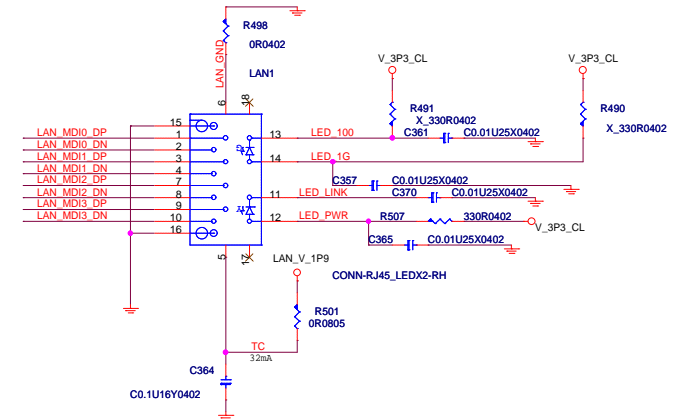


## SERIAL ATA CONNECTOR BLOCK

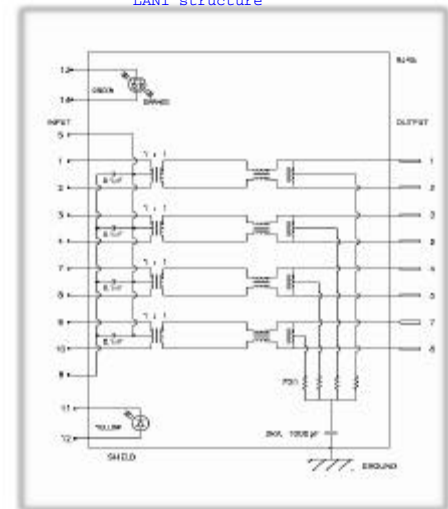




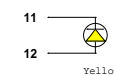
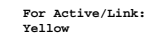
## LAN CONNECTOR



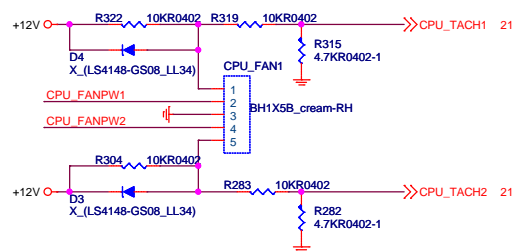
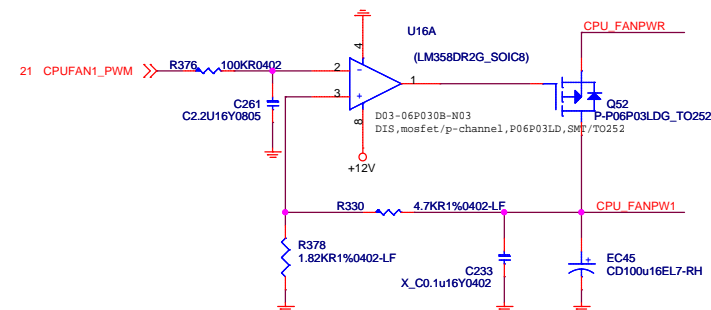
## LAN1 structure



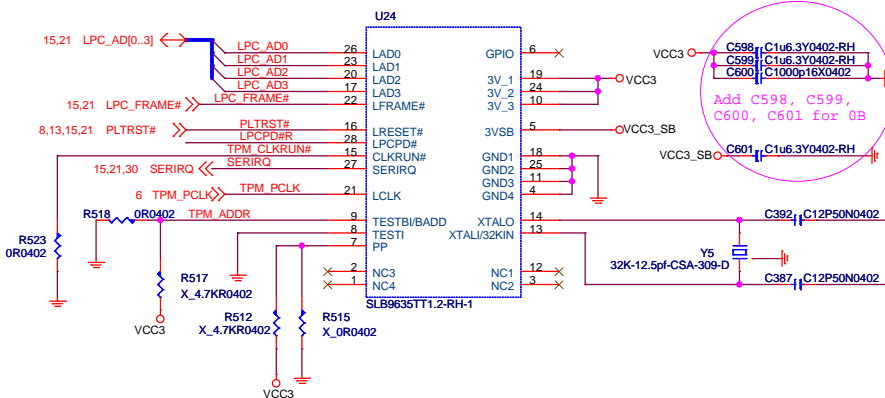
```
Speed LED Type
1000Mbps : Orange
100Mbps  : Green
10Mbps   : LED off
```








The four decoupling capacitors should be placed as short as possible to the respective 3V and 3VSB pins of the chip.



added R624 and reversed R623 for OC by Infineon' s suggestion on 06/09

TPM PCLK 1  
PLTRST# 3  
LPC AD0 5  
LPC AD1 7  
LPC AD2 9  
LPC AD3 11  
LPC FRAME# 13

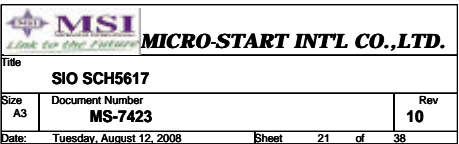
The diagram shows a circuit for pin 15,21, labeled LPCPD#. The pin is connected to a pull-up resistor R623 (10K R0402) which is connected to VCC3. The pin signal is labeled X 0R0402. The pin is also labeled LPCPD#R.

 <b>MICRO-START INT'L CO.,LTD.</b>	
Title	
TPM/FAN/LPC Debug Port	
Size	Document Number
Custom	MS-7423
Date:	Tuesday, August 12, 2008
Sheet	19 of 38
Rev	10



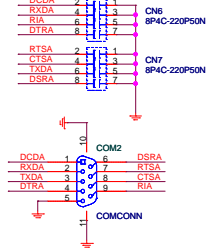
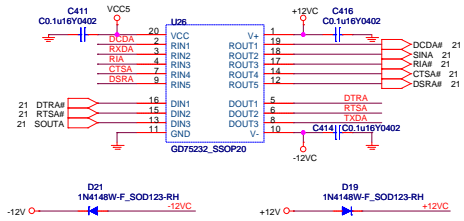




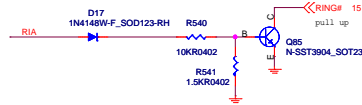




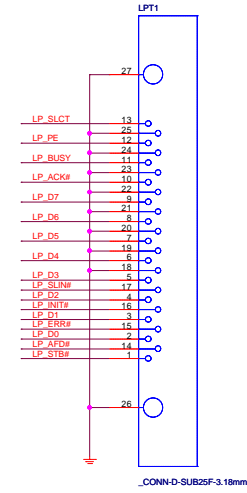
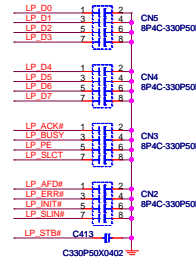
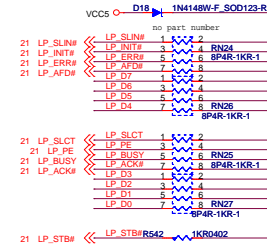
## SERIAL PORT 1



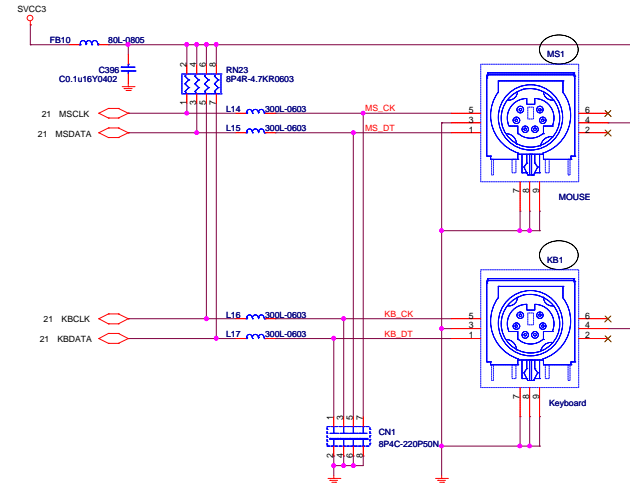
## Wake On Modem Header



## PARALLAL PORT

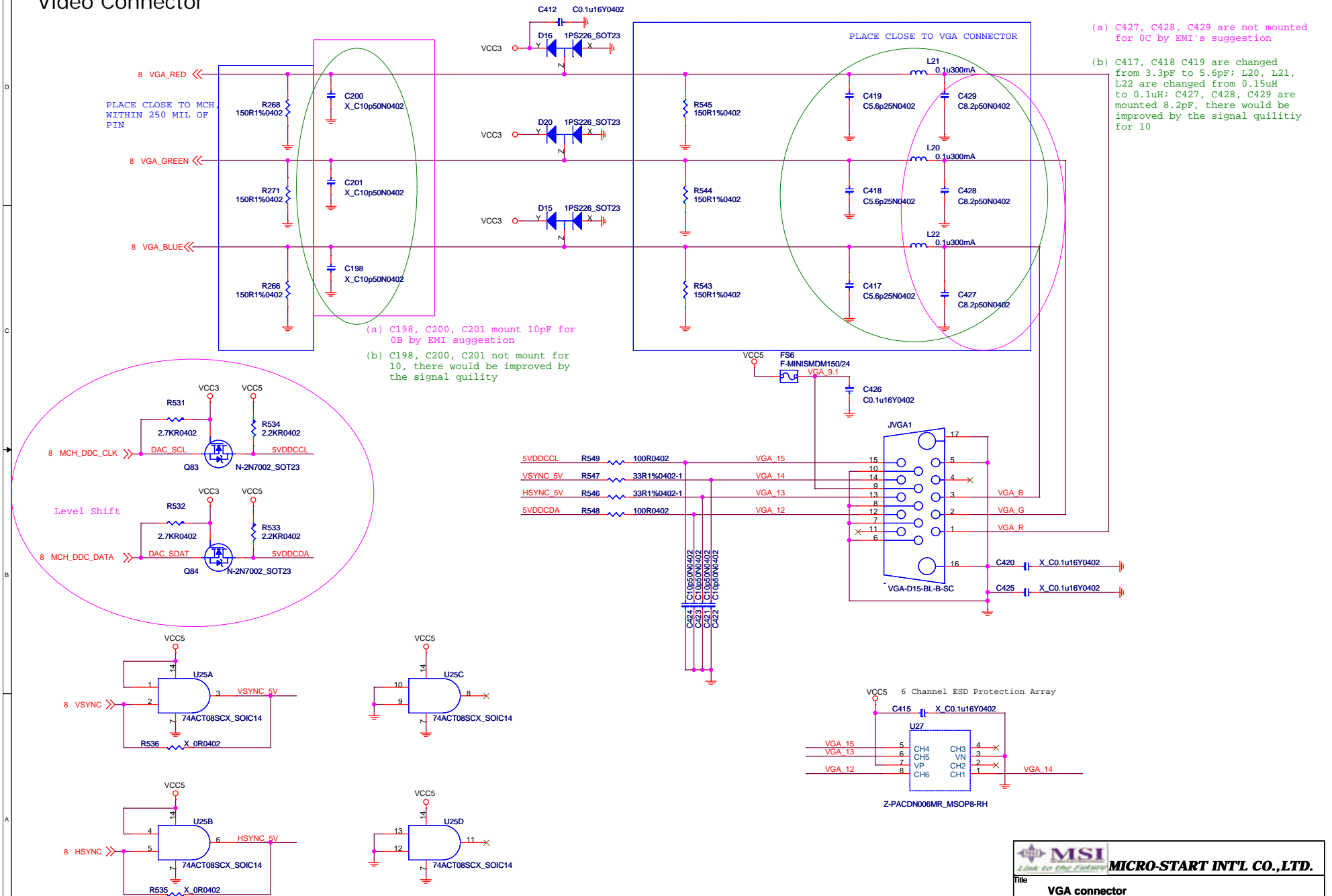


## PS2 KEYBOARD & MOUSE CONNECTOR



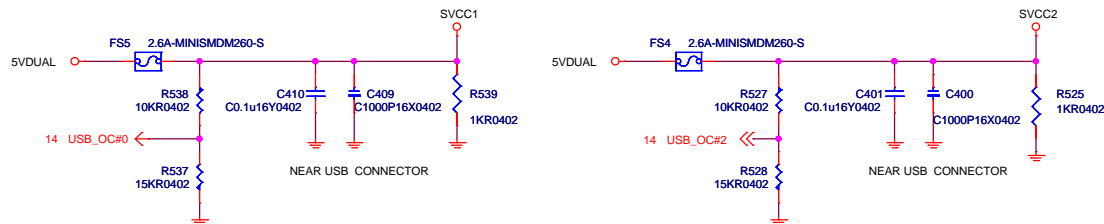


## Video Connector

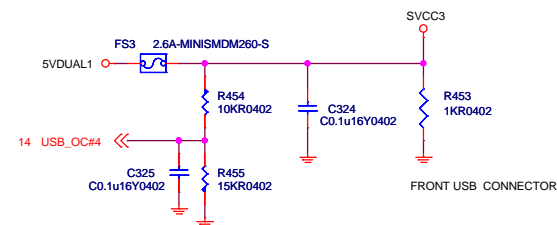




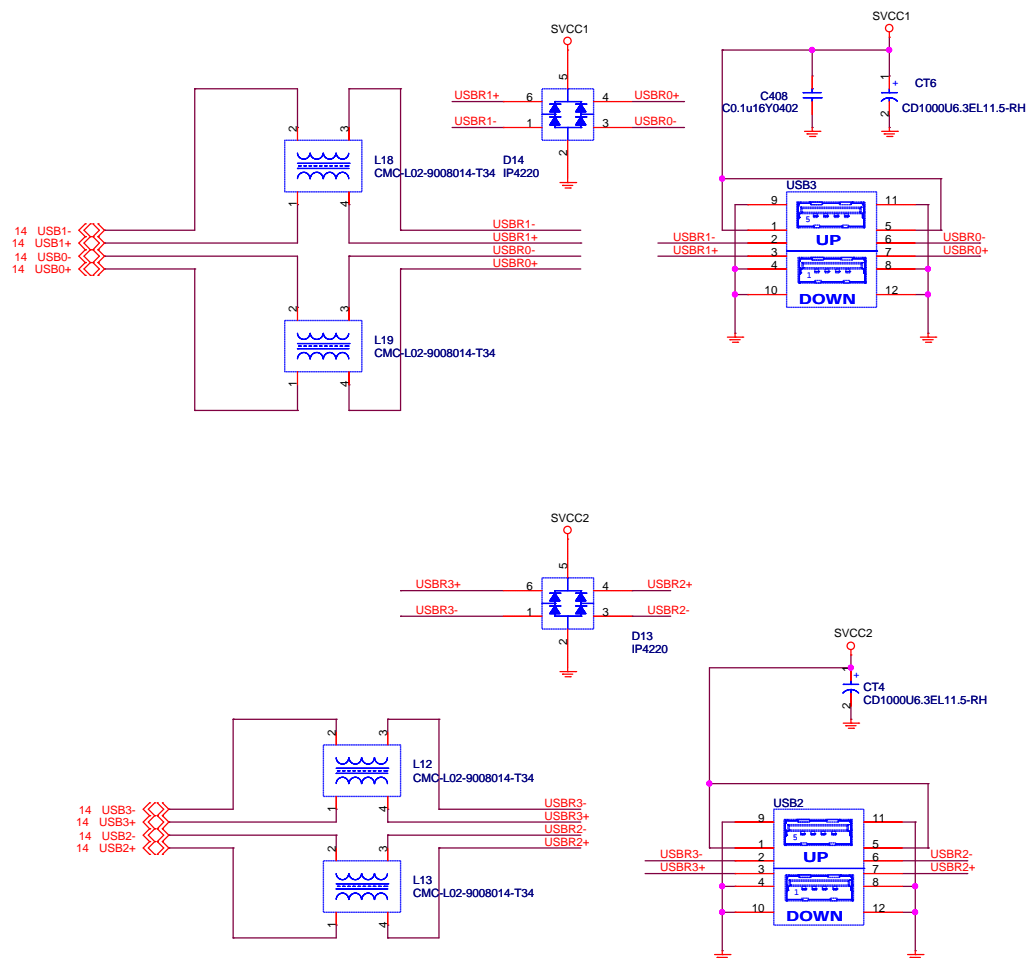
## POWER CIRCUIT FOR USB PORT 0,1,2,3



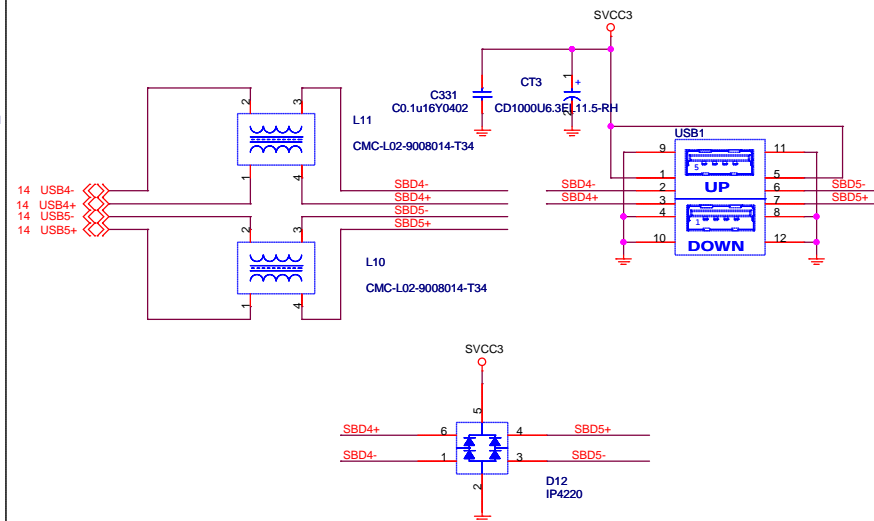
## POWER CIRCUIT FOR USB PORT 4,5



## REAR PANEL USB CONNECTOR FOR USB PORT 0,1,2,3



## FRONT PANEL USB CONNECTOR FOR USB PORT 4,5



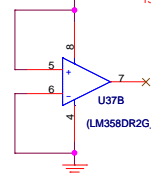
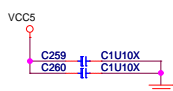


## VDIMM LINEAR OR PWM SELECT

VDIMM MODE	EXTRAM
LINEAR REGULATOR	PULL LOW
PWM REGULATOR	PULL HIGH

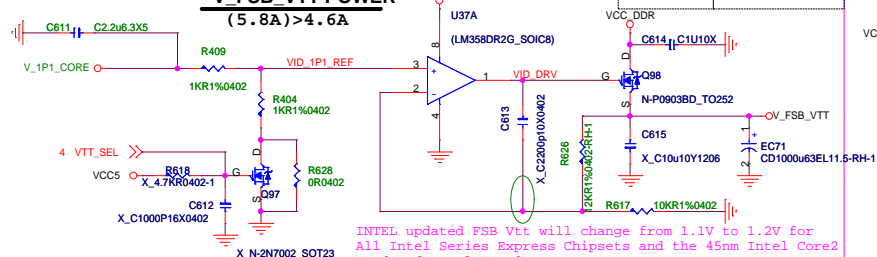
### 3VSB MODE SELECT

3VSB MODE	3VDDLDEC#
SINGLE MOSFET	PULL HIGH
DUAL MOSFET	PULL LOW



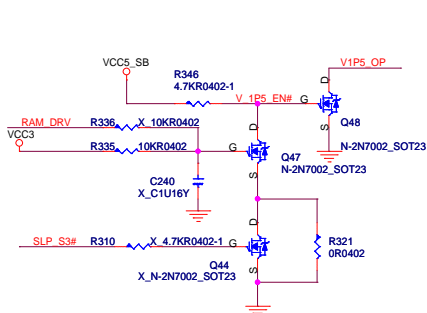
For 0C

C611 is changed from 2200pF to 2.2uF; R409 is changed from 2.7K ohm to 1K ohm 1%; R404 is mounted 1K ohm 1%; added 0ohm to R628; added 12Kohm 1% to R626; R617 is changed from 10Kohm to 10K ohm 1% by E0 stepping of CPU for 1.0

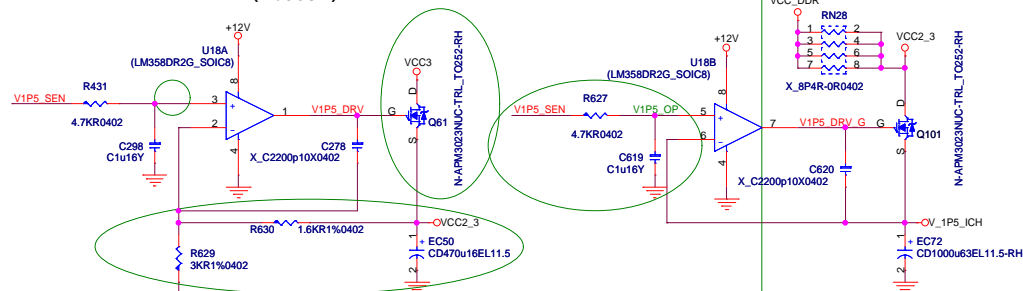
$$\frac{V_{FSB\_VTT} \text{ POWER}}{(5.8A)} > 4.6A$$


INTEL updated FSB Vtt will change from 1.1V to 1.2V for All Intel Series Express Chipsets and the 45nm Intel Core2 Quad and Intel Core2 Duo processors.

V1P5\_SEN S3 power sequency



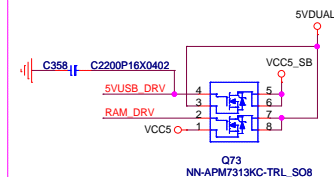
**ICH10 1.5V POWER**  
**(2.385A)**



There would be solved by CPUPWRGD glitch when S0 to S5 for 1.0 modification

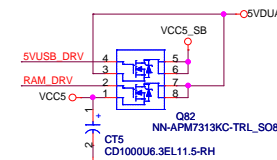
```
S5<-->S0: RAM_DRV go W/ SLP_S3#. (SLP_S3# active before VCC5)
S5<--> S0<-->S3: 5VUSB_DRV& RAM_DRV go W/ PWRGD_3V.
```

**5V DUAL Front Power**  
(2A)

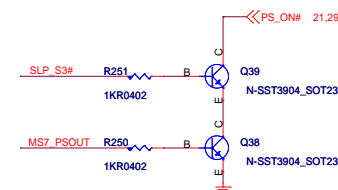


near USB      The same as ROPROS

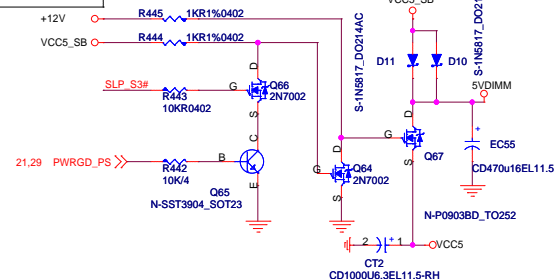
**5V DUAL Rear Power**  
**(2A)**



**PSON#**



## 5VDIMM

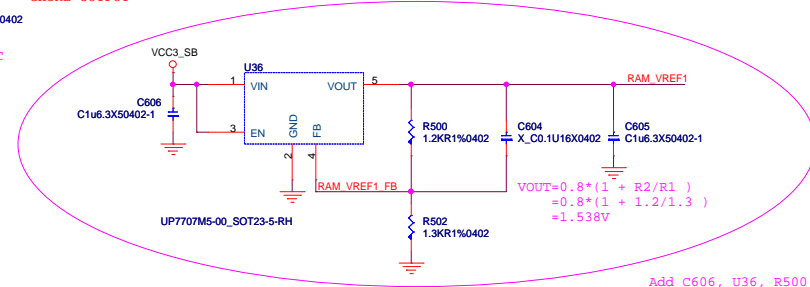


**MICRO-START INTL CO.,LTD.**

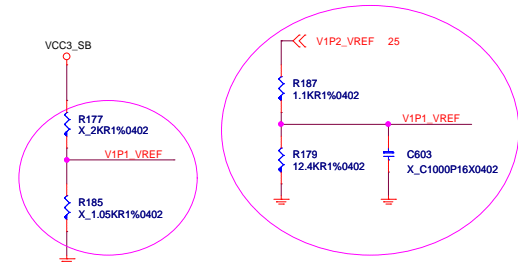
Title			
ACPI CONTROLLER MS7			
Size	Document Number		Rev
	MS-7423		10
Date:	Tuesday, August 12, 2008	Sheet	25 of 38



EC62 change from 1000uF to 820uF for 0B

[illegible]

Add C606, U36, R500, R502, C605, reserve C604 for 0B



R177, R185 not mount; mount 1.1K $\Omega$  to R187; mount 12.4K $\Omega$  to R179, reverse C603 for 0B



[illegible]

remove Q62, Q63 then add Q102 for 10

To avoid system might hang up issue,  
add Q100, R625 for 10 based on WW21MOW  
and WW23MOW

[illegible]

R456, C326, R457, R451, R452 not mount for 0B

Note:

- SLP\_S4#  
AMT Disable-->indicate ACPI S4 state,DRAM power off.
- AMT Enable-->not be asserted ACPI S4 state,DRAM power ON
- SLP\_M#  
AMT Enable SLP\_M#-->Control the overall power to Intel AMT during ACPI S3-S5.
- S4\_SATE#  
AMT Enable-->indication of ACPI S4 state

The diagram shows a power management circuit. At the top, there are two input pins: VCC5\_SB and V\_3P3\_CL. VCC5\_SB is connected to a resistor R389 (5.6KR0402), which is then connected to the gate of a MOSFET Q103 (NN-CMKT3904\_SOT363-6-RH). V\_3P3\_CL is connected to a resistor R400 (1KR1%0402), which is also connected to the gate of Q103. The drain of Q103 is connected to a node labeled MCH\_CLPWROK, which is also connected to a red arrow pointing to another MCH\_CLPWROK signal. This node is also connected to a capacitor C265 (X\_C1U16V) to ground. The source of Q103 is connected to a node labeled V\_1P1\_CL, which is also connected to a resistor R410 (10KR0402). This node is connected to a capacitor C272 (C1U16V) to ground. There is also a capacitor C275 (C4.7u6.3X50805) connected to ground. Below the diagram, the text reads: "remove Q57, Q58 and then add Q103 for 10".

remove Q57, Q58 and then add Q103 for 10



# Intersil 6334

## 3Phases

- (a) R191 is changed form 1.91K ohm 1% to 1.5K ohm 1% by vendor's suggestion for 0B
- (b) R191 is changed form 1.5K ohm 1% to 1.69K ohm 1% by vendor's suggestion for 0C

R232 pull up to change from V\_LPI\_CORE to V\_FSB\_VTT for 10

5.8 PSI#  
8 PSI#\_N

3 VCC\_VRM\_SENSE

3 VSS\_VRM\_SENSE

(a) C164 is changed form 22nF to 10nF by power team's suggestion for 0C

(b) C164 is changed form 10nF to 1nF by Intersil's suggestion for 10

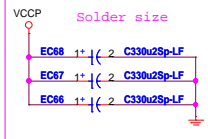
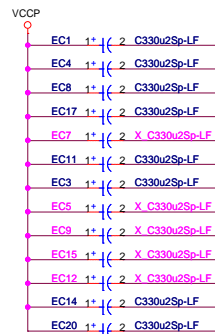
C126, C127, C129 are changed from 100pF to 68pF by vendor's suggestion for 0B

### ATX12V Power Connector

TDK  
NTCG104KF104FT

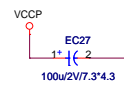
VR FAN TRIP: 1.69V ~ 80 degC  
VR HOT TRIP: 1.44V ~ 90 degC

### SP Capactors



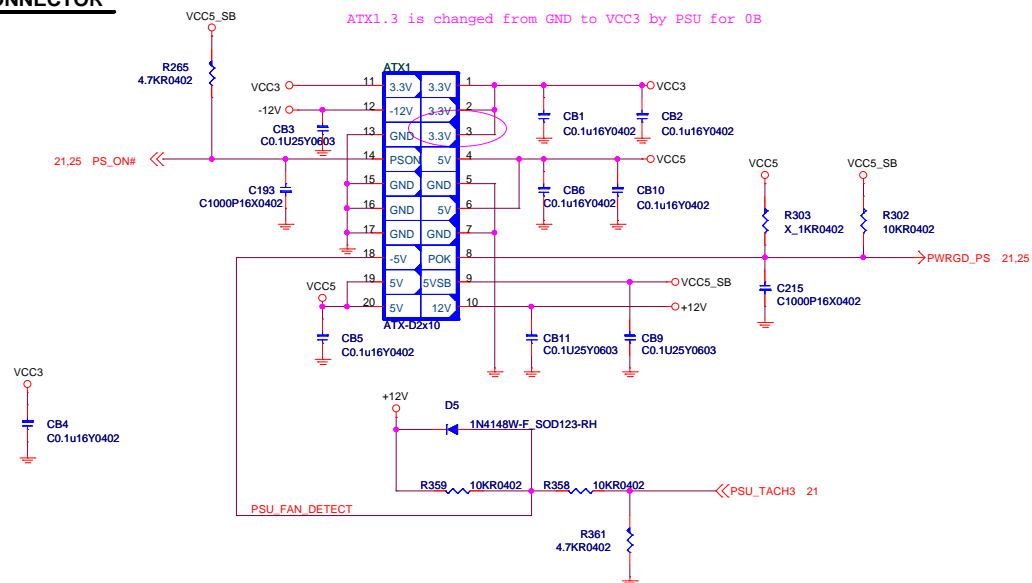
EC7, EC5, EC9, EC15, EC12 are mounted by power team's suggestion for 0C

### SP Capacitors





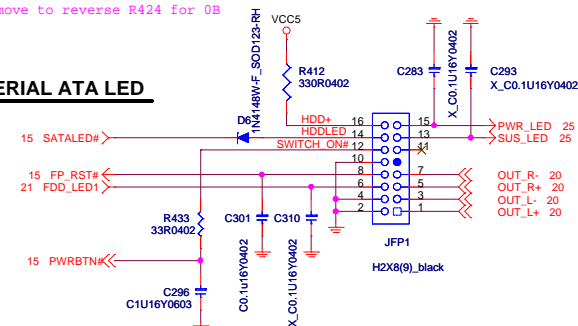
## ATX CONNECTOR



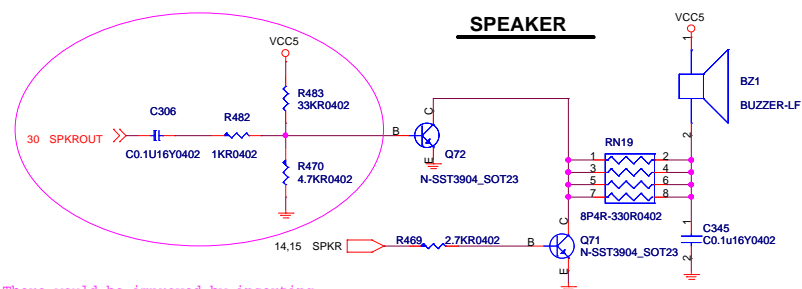
## Front Panel

remove to reverse R424 for 0B

## SERIAL ATA LED

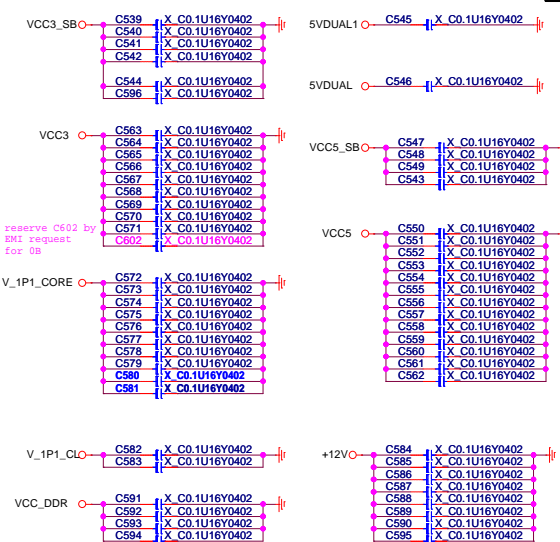


## SPEAKER




There would be improved by inserting some 32bits CardBus card

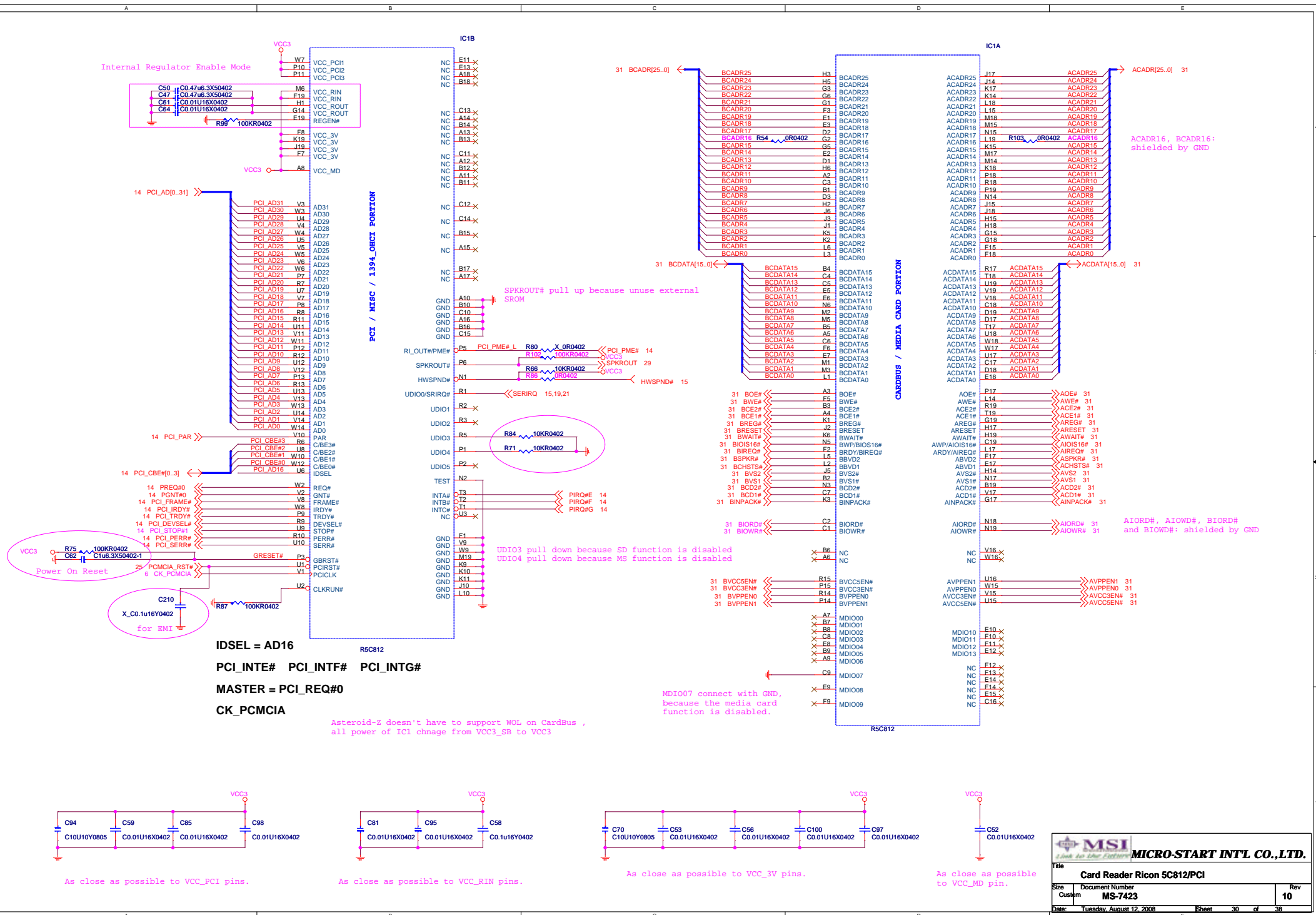
## EMI decoupling cap



reserve C616, C617, C618 by EMI request for 0C

 <i>Link to the Future</i>		<b>MICRO-START INTL CO.,LTD</b>	
Title			
<b>ATX/Front Panel</b>			
Size	Document Number		Rev
Custom	<b>MS-7423</b>		<b>10</b>
Date:	Tuesday, August 12, 2008	Sheet	29 of 38













## Manual Parts

JBAT1(1-2)1



JMP/GREEN/A

J4(1-2)1



JMP/GREEN/A

JCH1(1-2)1



JMP/GREEN/A

BAT1\_X2



PCB1



PCB-MS-7423N1-10

BIOS\_LABEL1



BIOS\_LABEL1

LAB1



Asteroid-S2

X\_MODEL\_LABEL

U13\_HS2  
H1X3[2]M\_BLACK-RH-2

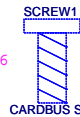
U13\_HS3  
H1X3[2]M\_BLACK-RH-2

U13\_HS2 & U13\_HS3 change to  
the same Asteriod-S3 by mechanical request on 04/16

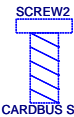
U15\_HS1



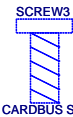
NB\_HEATSINK



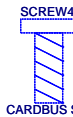
CARDBUS SCREW



CARDBUS SCREW



CARDBUS SCREW



CARDBUS SCREW

## Audio Jack EMI solution



GASKET



GASKET



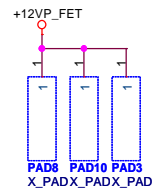
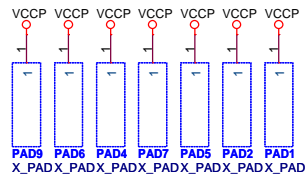
CLAMP1



CLAMP2

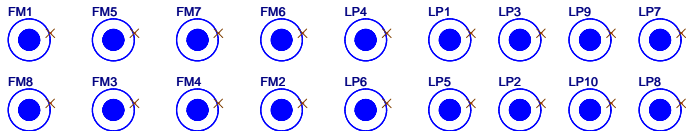


CLAMP3

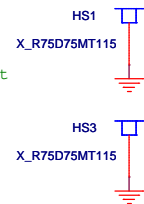


J1 and J2 are changed to standard footprint  
by factory request for 10

## Optics Orientation Holes

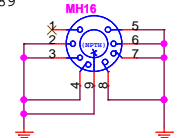


## Simulation




For thermal reserved

for power cable holder and FP:  
HOLES315D189



added HS5 & HS6 by mechanical  
request for 0B on 04/25

 <b>MICRO-START INTL CO.,LTD.</b>			
Title <b>Manual Parts</b>			
Size B	Document Number <b>MS-7423</b>		Rev <b>10</b>
Date: Wednesday, August 13, 2008	Sheet 32	of 38	



# ICH10

GPIO Pin	Type	Default	Function	Power	MUXED/ UNMUXED	Pin-out
GPIO 0	I/O	GPI	BMBUSY# function, Pull-up to VCC3 with 10K	VCC3	MUXED	N7
GPIO 1	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3	MUXED	AK21
GPIO 2	I/O	GPI	PIRQ#E pull-up to VCC3 with 8.2K	VCC3		K6
GPIO 3	I/O	GPI	PIRQ#F pull-up to VCC3 with 8.2K	VCC3		L7
GPIO 4	I/O	GPI	PIRQ#G pull-up to VCC3 with 8.2K	VCC3		F2
GPIO 5	I/O	GPI	PIRQ#H pull-up to VCC3 with 8.2K directly	VCC3		G2
GPIO 6	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3	MUXED	AH22
GPIO 7	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3	MUXED	AK23
GPIO 8	I/O	GPI	DDR3_PWROK function , Pull-up to VCC3_SB with 10K	VCC3_SB	UNMUXED	A20
GPIO 9	I/O	GPO/WOL	WOL_ENABLE, pull-down with 100K	VCC3_SB	MUXED	A18
GPIO 10	I/O	GPI	Pull-up to VCC3_SB with 10K directly	VCC3_SB	MUXED	C17
GPIO 11	I/O	SMBALERT#	SMB_ALERT# pull-up to VCC3_SB with 10K	VCC3_SB		C16
GPIO 12	I/O	GPO	LAN_DISABLE connect to LAN Boazman	VCC3_SB	UNMUXED	A8
GPIO 13	I/O	GPI	SIO_PME# connect to SIO, pull-up VCC3_SB with 10K	VCC3_SB	UNMUXED	A19
GPIO 14	I/O	GPI	Pull-up to VCC3_SB with 10K directly	VCC3_SB	MUXED	A9
GPIO 15	I/O	GPO	PCI_STOP# connect to CLK Gen	VCC3_SB	MUXED	C15
GPIO 16	I/O	GPO	* PANEL_DETECT, pull up to VCC3 with 10Kohm	VCC3	UNMUXED	M2
GPIO 17	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3	MUXED	AH21
GPIO 18	I/O	GPO	GTLREF GPO	VCC3	UNMUXED	K1
GPIO 19	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AE20
GPIO 20	I/O	GPO	GTLREF GPO	VCC3	UNMUXED	AF5
GPIO 21	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AK25
GPIO 22	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3	MUXED	AJ24
GPIO 23	I/O	LDRQ1#	NC	VCC3	MUXED	J3
GPIO 24	I/O	GPO	NC	3.3V_SB	MUXED	A14
GPIO 25	I/O	GPO	CPU_STOP# connect to CLK Gen	3.3V_SB	UNMUXED	B18
GPIO 26	I/O	GPO	S4 STATE# connect to SIO	3.3V_SB		C11
GPIO 27	I/O	GPO	* NC	3.3V_SB		A11
GPIO 28	I/O	GPO	NC	3.3V_SB		G18
GPIO 29	I/O	OC5#	OC#4 connect to USB connector	3.3V_SB		N1
GPIO 30	I/O	OC6#	OC#4 connect to USB connector	3.3V_SB		N5
GPIO 31	I/O	OC7#	OC#4 connect to USB connector	3.3V_SB		M1
GPIO 32	I/O	GPO	PROCHOT#, THERM# GPO	VCC3	UNMUXED	K2
GPIO 33	I/O	GPO	ME FPRG; Pull-up to VCC3 with 4.7K through JC11 Jumper. (Default)	VCC3	UNMUXED	AF6
GPIO 34	I/O	GPO	HWSPPND# connect to R5C812	VCC3	UNMUXED	AH5
GPIO 35	I/O	GPO	NC	VCC3		L1
GPIO 36	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AE21
GPIO 37	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AE22
GPIO 38	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AK24
GPIO 39	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AH23
GPIO 40	I/O	OC1#	OC#0 connect to USB connector	3.3V_SB		N3
GPIO 41	I/O	OC2#	OC#2 connect to USB connector	3.3V_SB		P7
GPIO 42	I/O	OC3#	OC#2 connect to USB connector	3.3V_SB		R7
GPIO 43	I/O	OC4#	OC#4 connect to USB connector	3.3V_SB		N2
GPIO 44/45	I/O	OC8/9#	OC#4 connect to USB connector	3.3V_SB		P3/R6
GPIO 46/47	I/O	OC10/11#	OC#4 connect to USB connector	3.3V_SB		T7/P1
GPIO 48	I/O	GPI	pull-up VCC3 with 10K directly	VCC3		AD20
GPIO 49	I/O	GPO	NC	VCC3		AJ25
GPIO 50	I/O	REQ1#	REQ1 pull-up to VCC5 with 2.7K directly	VCC5	MUXED	G13
GPIO 51	I/O	GNT1#	NC	VCC3	MUXED	A7
GPIO 52	I/O	REQ2#	REQ2 pull-up to VCC3 with 8.2K directly	VCC5	MUXED	F13
GPIO 53	I/O	GNT2#	NC	VCC3	MUXED	C7
GPIO 54	I/O	REQ3#	REQ3 pull-up to VCC5 with 2.7K directly	VCC5	MUXED	G8
GPIO 55	I/O	GNT3#	NC	VCC3	MUXED	F7
GPIO 56	I/O	GPI	CLR_PW, pull-up to VCC3_SB with 10K.	3.3V_SB	MUXED	F16
GPIO 57	I/O	GPI	Pull-up to V_3P3_CL with 1K	3.3V_SB	MUXED	C12
GPIO 58	I/O	SPI_CS1	NC	3.3V_SB	MUXED	F23
GPIO 59	I/O	OC0#	OC#0 connect to USB connector	3.3V_SB		P5
GPIO 60	I/O	LINKALERT#	LINKALERT# pull-up to VCC3_SB with 10K	3.3V_SB		F18
GPIO 61	I/O		LPCPD# connector to SIO	3.3V_SB		R1
GPIO 62	I/O		NC	3.3V_SB		R5
GPIO 72	I/O		BATTLOW# pull-up to VCC3_SB with 10K ohm	3.3V_SB		C13

## SIO - SMSC-5617C Configuration

PIN NAME	PIN#	USAGE	Input/Output
GP41	77	SIO_PME#	OUTPUT
GP25	30	SMBCLK	INPUT
GP26	29	SMBCLK_ISO	INPUT
GP35	28	SMBDATA	OUTPUT
GP42	27	SMBDATA_ISO	OUTPUT

## PCI Configuration

DEVICE	MCP1 INT Pin	REQ# /GNT#	IDSEL	CLOCK
Ricoh R5C812	PIRQ#E PIRQ#F PIRQ#G	PREQ#0 PGNT#0	AD16	CK_PCMCIA

## PCI\_RST# DISTRIBUTION

SOURCE	PCIRST#	LOAD
ICH10	PCMCIA_RST#	Ricoh R5C812
	PCIRST_ICH10#	MS7
MS7	MINI_PCIE_RST#	MINI PCIE
	PLTRST#	TPM
	RSMRST#	ICH10
NB	H_CPUURST#	CPU

## DDR III DIMM Config.


DEVICE	ADDRESS	CLOCK
DIMM 1	A0H	SCLK_A0 / SCLK_A0#
		SCLK_A2 / SCLK_A2#
DIMM 2	A4H	SCLK_B0 / SCLK_B0#
		SCLK_B2 / SCLK_B2#

## Jumper Setting

JBAT1	(1-2)Normal	(2-3)Clear CMOS
JCI1	(1-2)Normal	(2-3)ME Disable for FPROG
J4	(1-2)short: Normal	(1-2)Open: Clear PW

## SMBus Distribution

SMBus	Power	Load
SMBCLK	VCC3_SB	SIO, ICH10, MINI PCI EXPRESS
SMBCLK_ISO	VCC3	DIMM, CLK GEN, MS7

 <b>MICRO-START INT'L CO., LTD.</b>	
Title <b>GPIO MAP</b>	
Size	Document Number
Custom	<b>MS-7423</b>
Date: Friday, July 18, 2008	Sheet 33 of 38
Rev <b>10</b>	



LGA775-CPU		
0.8375V - 1.6000V Core	-	84A
1.1V FSB Vtt	-	4.6A

Eaglelake (GMCH)		
1.1V FSB_VTT	-	1.2 A
1.1V Core TBD (USE LB)	-	13.8A
1.1V DMI/PCI Exp.	-	2.47 A
1.5V VCC_DDR	-	3.33A
1.5V VCC_SMCLK	-	350mA
3.3V VCCA_DAC	-	66 mA
3.3V VCC33	-	15.8mA
1.1V Vcc CL	-	4.3A

ICH10		
1.1V DMI	-	41 mA
1.1V Core	-	1.16A
1.5V_A USB/SATA/PLL	-	1.652A
1.5V_B PCI Exp.	-	0.646A
VCCRTC	-	6 uA
3.3V CL	-	19 mA
1.5V GbE LAN	-	87 mA
3.3V VccSus3_3	-	200mA
3.3V Vcc3_3	-	308mA
3.3V 10/100 LAN	-	19 mA
3.3V GbE LAN	-	1 mA
3.3V HDA	-	32 mA
3.3V SusHDA	-	33 mA

HD Audio ALC262VD		
3.3V AUDIO	-	40mA
5V AUDIO	-	200mA

IDTCV184-2		
3.3V VDD_48/PCI/REF	-	250mA
0.3V-1V CPU/SRC/DOT/PLL	-	80mA

Boazman GbE		
3.3V_SB I/O & LED	-	15.5mA
1.8V AVDD	-	418.2mA
1.0V Core	-	277.2mA

ISL6334		
VCCP VRD11.1	-	0.8375V-1.6000V
3-Phase Switch	-	

W83310DS		
VTT_DDR	-	0.75V Linear 0.83A

MS11+ SW-Power		
VCC_DDR	-	1.5V PWM 13.86A

MS11+ SW-Power		
V_1P1_CORE	-	1.1V PWM 23.27A

MS7 Controller		
V_1P1_CL	-	1.1V Linear 3A

MS7 Controller		
V_1P5_ICH	-	1.5V Linear 2.385A
VCC3_SB	-	3.3V Linear 3.96A
5VDUAL1	-	5V Switch 4.367A
5VDIMM	-	5V Switch 8.29A

DDRIII x2 & TERMINATOR		
0.75V VTT_DDR	-	1.2A
1.5V VCC_DDR (S0,S1)	-	3.6A
1.5V VCC_DDR (S3)	-	TBDmA

LVDS		
2.5V	-	340mA
+3.3V	-	85mA

Mini PCI_E x1 slot		
+3.3Vaux	-	1100mA
1.5V	-	375mA

PCMCIA dual slot		
5V	-	1A
+3.3V	-	375mA

USB x 6		
+5V (S0,S1)	-	3A
+5V (S3)	-	20mA

PS2		
+5V (S0,S1)	-	345mA
+5V (S3)	-	2.0mA

5VAudio		
+5VR	-	500mA

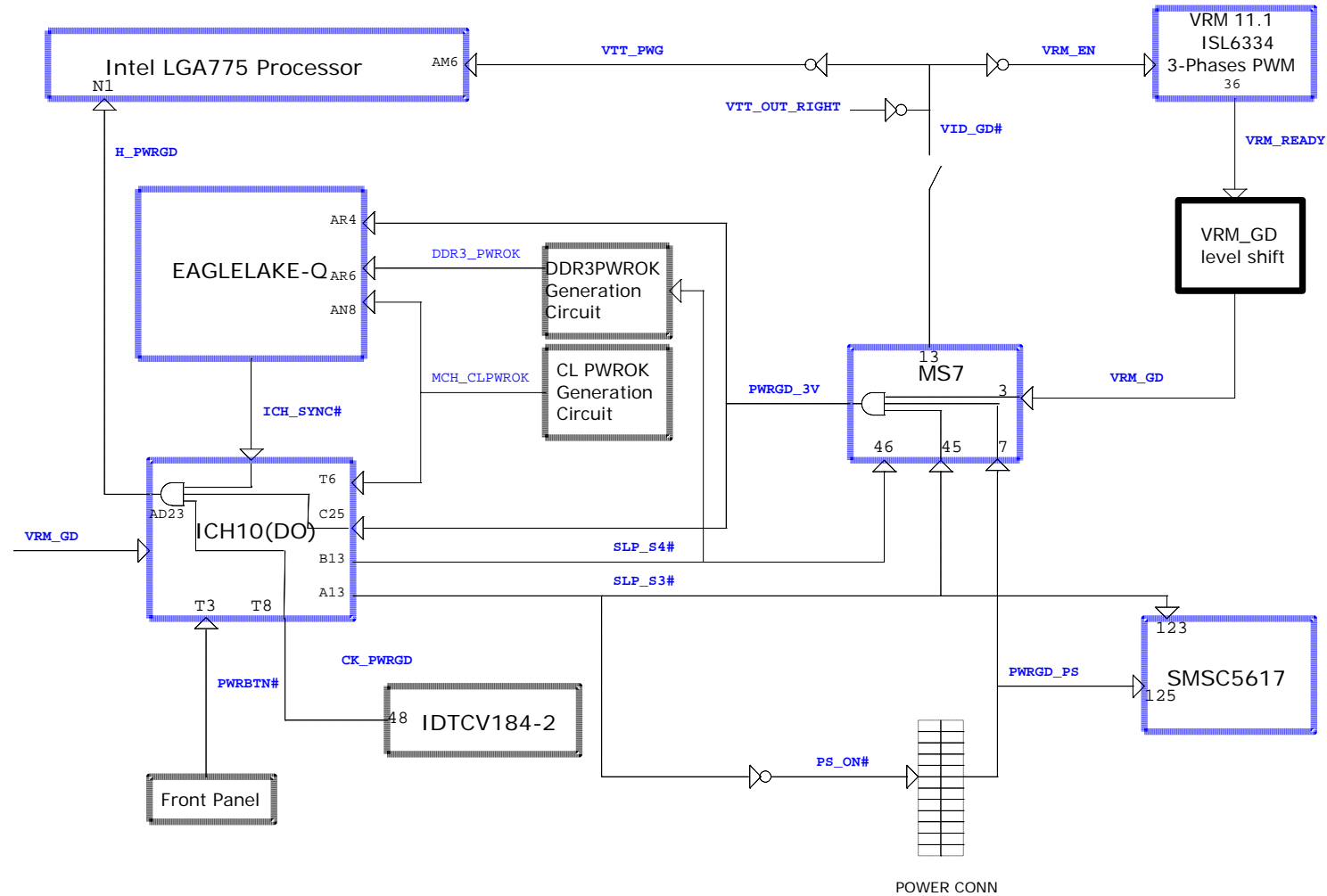
+12V		
ATX 2x2	-	

ATX POWER			
+5V (10A)	+3.3V (12A)	+5VSB (10A)	+12V (12A)

PSU: DPS-200PB-168 A REV:50F

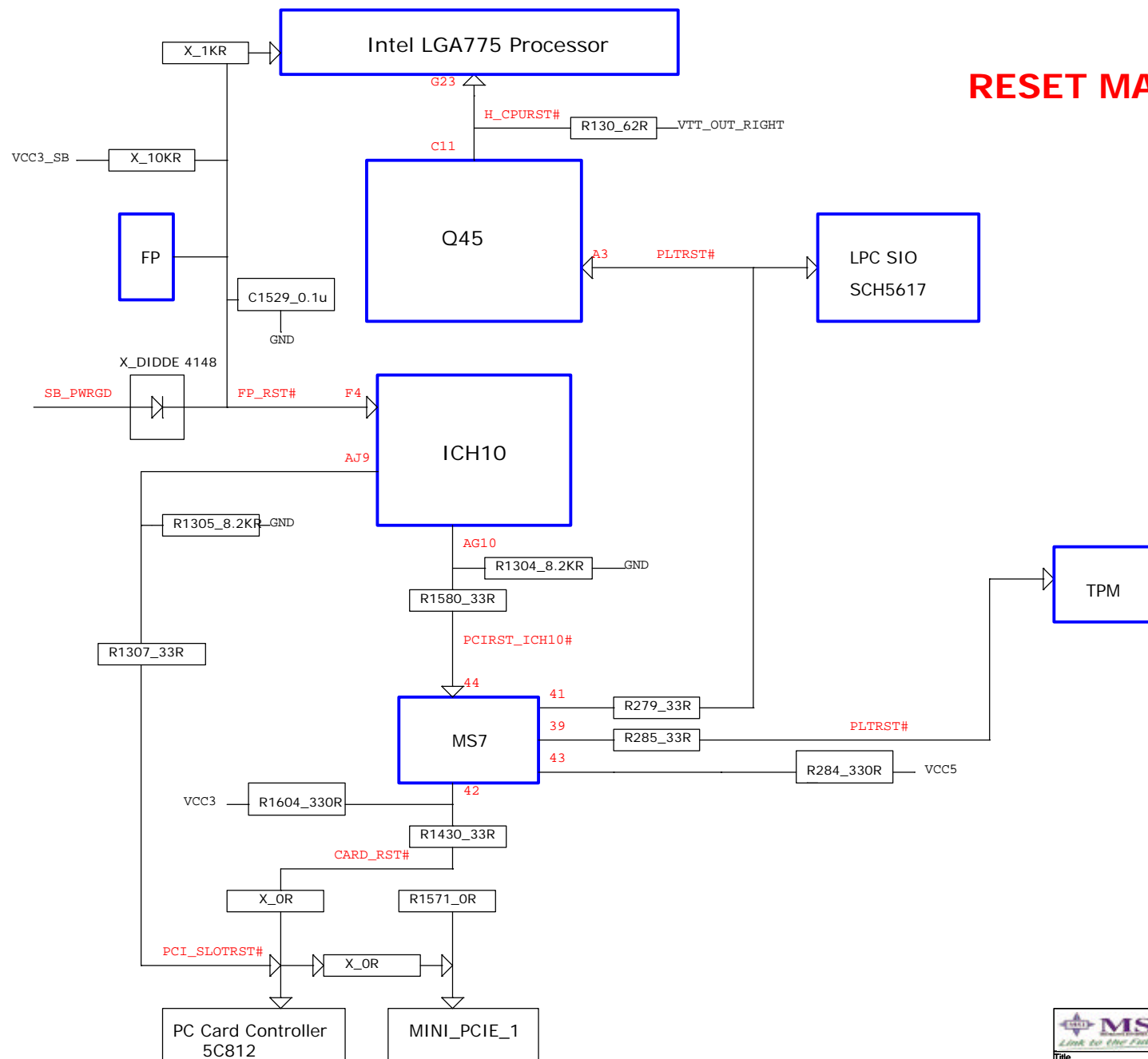


# PWROK MAP





# RESET MAP





0A

(1) Remove the AC Coupling Capacitor(C306,C307) on Rx signal line. Because these Capacitor were mounted on Rxsignal line in MINI Card module board from NECP comment on page 17 on 2/20

0B

(1) Remove R152 and PM\_DPRSTR\_N(net) connect directly to U7.T2 on page 3

(2) R109, R111 not mount because they have unused on page 3

(3) U7.A23, U7.B23, U7.C23 change to test point on page 4

(4) Remove L1, R100, C87, C80, C92(they have unused), add Q92, R612, R613( add level shift between PROCHOT# and ICH10 (GPIO32) for NECP economy mode) on page 4

(5) Remove Q34, Q36, add Q91(unify the materials) on page 4

(6) C28, C29 are changed from 27pF to 47pF on page 6

(7) EC60 change from 1000uF to 820uF and EC58 mount 820uF on page 8

(8) R158 no mount, Q27 mount, remove R142, add Q34 (Intel PSI# design update)on page 8

(9) Remove Q54, Q56, add Q36, R385 mount(Intel suggestion), C262 change from 1uF to 12nF(Intel suggestion) on page 9

(10) C287 change from Y5V to X7R, C290 change from 0603 type/Y5V to 0402 type/X7R (follow Intel design)on page 9

(11) Remove R257 and L7 change from 10uH to 0ohm on page 10

(12) C44, C45 change from 27pF to 33pF on page 13

(13) Support Danbury, R390 mount 10Kohm on page 14

(14) Remove R409(it has unused), R332(immediately); R308 mount 33ohm(use ICH10 DRAMPWROK function pin); add GPIO\_32(net); R242, R245not mount (Intel suggestion) , R398 not mount(GPIO18 is already output function, don't need to pull-up); reserve C307(RC timing) on page 15

(15) C403, C404, C405 mount 0.1uF on page 18

(16) Added the four decoupling capacitors( C598, C599, C600, C601 ) should be placed as short as possible to the respective 3Vand 3VSB pins of the chip on page 19

(17) Add LPC debug port at JLPCL on page 19

(18) Solving the audio become to mute, rename to AC\_RST# (net) on page 20

(19) C528 is changed to T34(vendor) by buyer request on page 20

(20) Remove R500, R502(because they have unused), add D25(Due to Peci\_REQUEST have leakage, SMSC have workaround to add a diode to avoid )on page 21

(21) remove R492(immediately) and C367 change from 270pF to 220pF(the same as LE) on page 21

(22) Remove C224 on page 25

(23) EC62, EC63 change from 1000uF to 820uF ; EC61 mount 820uF; R437 & R439 not mount; Add C606, U36, R500, R502, C605, reverse C604; R177, R185 not mount; mount 1.1K $\Omega$  to R187; mount 12.4K $\Omega$  to R179, reverse C603; CHOKE6, CHOK5, COIL1, COIL2 change for transient and noise on page 26

(25) VRM solution change from DR.MOS to PowerPack(the same as LE), pls refer to page 28

(26) U13\_HS2 & U13\_HS3 are changed to the same AZ-S3 by mechanical request on 04/16

(27) R607, R608 are change from 6.8Kohm $\Omega$  to 18Kohm $\Omega$ , R572, R581 are change from 20Kohm $\Omega$  to 13Kohm $\Omega$  by customer request on page 20 on 04/17

(28) R140 change 0603 type to 0805 type(unify the materials) ; R137, R138, R139 are change from 4.7Kohm  $\Omega$  to 6.19.Kohm  $\Omega$  ; C126, C127, C129 are changed from 100pF to 68pF ; R191 is changed form 1.91K ohm  $\Omega$  to 1.5K ohm  $\Omega$  by vendor's suggestion on page 28

(29) U15 stepping change from A1 to A3 on page 7~11

(30) U13\_HS2 & U13\_HS3 change to the same Asteriod-S3 by mechanical request on 04/16

(31) Asteroid-Z doesn't have to support WOL on CardBus , all power of ICL chnage from VCC3\_SB to VCC3 , remove Q25, R166, C142, Q22 from NECP comment on page 30 & 31 on 04/18

(32) ATX1.3 is changed from GND to VCC3 by PSU , remove to reverse R424 for 0B on page 29

(33) C189&C190 change from Y5V to X7R on page 14

(34) C381&C383 change from Y5V to X7R on page 18

(35) U30, U32 are changed from SCHMITT-TRIGGER to BUFFER and are added R615, R614, R616 by customer request on page 20 on 4/22

(36) R387 and R388 not mount on page 9

(37) remove R404(reserved) on page 15

(38) remove to reserve R100 and R166 from CH7308B's datasheet rev2.1 on page 13

(39) C198, C200, C201 are mounted 1pF by EMI suggestion on page 23

(40) reserved decoupling cap to C602 by EMI request on page 29

(41) added HS5 & HS6 by mechanical request on page 32 on 04/25

(42) Add EC70 near CPU on page 26

(43) U13 stepping change to B0 on page 14 ~ 16


(44) EC2, EC6, EC10, EC13, EC18 are changed to a height of 11mm by mechanical & thermal request on page 13

(45) reserved C607,C608, C609, C610 by checklist request on page 21

(46) add FS7 by checklist request on page 13

(47) R3, Q1, Q2, R5, Q3 not mount because pin 27 of LCD\_1 is NC and BIOS no support S1 mode on page 13

A

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0B

- (48) R601 and R606 are change from 47ohm 5% to 51ohm 1% by customer request on page 20 on 05/14  
(49) R298, R350 not mount (pin 27 of LCD\_1 is NC pin) and R350 not mount(BIOS no support S1 mode) on page 15  
(50) R456, C326, R457, R451, R452 not mount on page 27

0C

- (51) Power name change from V\_1P1\_CORE to V\_FSB\_VTT on page 3, 4, 7, 10, 11  
(52) C138 mount 220pF on page 4  
(53) R279 change from 1Kohm to 1.02Kohm on page 8  
(54) D25 change from 4148 to 5817 on page 21  
(55) Intel updated FSB Vtt will change from 1.1V to 1.2V for all Intel Series Express Chipsets and the 45nm Intel Core2 Quad and Intel Core2 Duo processors on page 25  
(56) Due to V\_FSB\_VTT become to 1.2V ,VTT\_DDR POWER increase to 19.66 A, so add a low size MOS(Q99) for DDR POWER on page 26  
(57) Added R624 and reversed R623 for 0C by Infineon' s suggestion on page 19 on 06/09  
(58) Remove R365 because of unuse on page 10  
(59) Reserve C616, C617, C618 by EMI request on page 29  
(60) Intel recommends using a pull up resistor of 100ohm (R391) to VCC5\_SB together with the 1uF X7R capacitor (C268). The change is to avoid a high ramp up rate on 5VSB (V5REF\_SUS) from WW23 MOW on page 16  
(61) R607 and R608 are change from 18Kohm%1 to 13Kohm%1 ; R601 and R606 are change from 51ohm 1% to 62ohm 1% by customer request on page 20 on 06/18  
(62) C427, C428, C429 are not mounted by EMI's suggestion on page 23  
(63) R191 is changed form 1.5K ohm 1% to 1.69K ohm 1%; C164 is changed form 22nF to 10nF; R137, R138, R139 are change from 6.19Kohm 1% to 9.1Kohm 1%; R196 is chnaged from 20Kohm 1% to 34.8Kohm 1%; C155 is changed from 22pF to 10pF; R180 is changed from 200 ohm to 402 ohm 1%; EC7, EC5, EC9, EC12 are mounted by power team's suggestion on page 28  
(64) R420 is changed from 1K ohm 1% to 750 ohm 1% ; R230 is changed from 1K ohm 1% to 402 ohm 1% by power team's suggestion on page 26

10

- (65) To avoid system might hang up issue, add Q100, R625 based on WW21MOW and WW23MOW on page 15 and page 27  
(66) U30 is changed from BUFFER to SCHMITT-TRIGGER by customer request on page 20 on 6/19  
(67) C164 is changed form 10nF to 1nF by Intersil's suggestion on page 28  
(68) The F/W of U24 is changed from 1.02 to 3.16 on page 19  
(69) C611 is changed from 2200pF to 2.2uF; R409 is changed from 2.7K ohm to 1K ohm 1%; R404 is mounted 1K ohm 1%; added 0ohm to R628; added 12Kohm 1% to R626; R617 is changed from 10Kohm to 10K ohm 1% by E0 stepping of CPU on page 25  
(70) R382 not mount; R611 mount on page 25  
(71) R381 not mount; recovery R365 and reverse C622 on page 10  
(72) Add R629, R630 R627, C619, Q101, EC72; reverse RN28, C620; Q61 change from 0903 to 3023; EC50 change from 1000uF to 470uF on page 25  
(73) net(PANEL\_DETECT) change from GPIO27 to GPIO16 and R350 mount 10Kohm on page 15  
(74) C374 and C597 mount 0.1uF by EMI request on page 20 on 08/01  
(75) JCI1.1 is change from GPIO\_33\_H to NC and JCI1.2 pull up VCC3 with R425 on page 15  
(76) Reversed R631 by customer request because Asteroid-Z doesn't support WOL on WLAN card on page 17 on 8/5  
(77) C198, C200, C201 not mount; C417, C418 C419 are changed from 3.3pF to 5.6pF; L20, L21, L22 are changed from 0.15uH to 0.1uH; C427, C428, C429 are mounted 8.2pF, there would be improved by the signal quility on page 23  
(78) remove R208, R122, R129, R189, R109, R111 because they are unused on page 3  
(79) remove R131, R145, net(TP\_CPU\_G1) because they are unused on page 5  
(80) Q34.D swap with Q34.S on page 8  
(81) remove C291 because C288(decoupling cap) should be placed as close as possible to DDR\_VREF pin of GMCH on page 9  
(82) remove R569, add CP4 ;R381 not mount; add R365,C622, R569; reserve R632 on page 10  
(83) remove net(CPU\_TMPA and VTIN\_GND) on page 21  
(84) remove R356, C245, R338, C243 because they are unused ;reserve R438 on page 25  
(85) remove R438 because it is unused on page 26  
(86) remove Q62, Q63 then add Q102; remove Q57, Q58 then add Q103 on page 27  
(87) R232 pull up to change from V\_1P1\_CORE to V\_FSB\_VTT on page 28  
(88) U13.AH28 and U13.AJ30 connect to change from VTT\_OUT\_RIGHT to V\_FSB\_VTT on page 16  
(89) J1 & J2 are changed to STD library by factory request on page 32

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